EUROPEAN COMMISSION

Brussels, 10.1.2025
C(2025) 193 final

PUBLIC VERSION

In the published version of this decision, some information has been omitted pursuant to Article 17(2) of Council Regulation (EC) No 139/2004 concerning non-disclosure of business secrets and other confidential information. The omissions are shown thus […]. Where possible the information omitted has been replaced by ranges of figures or a general description.

Synopsys, Inc.
675 Almanor Avenue
Sunnyvale, CA 94085
United States of America

Subject: **Case M.11481 – SYNOPSYS / ANSYS**
Commission decision pursuant to Article 6(1)(b) in conjunction with Article 6(2) of Council Regulation No 139/2004[1] and Article 57 of the Agreement on the European Economic Area[2]

Dear Sir or Madam,

(1) On 11 November 2024, the European Commission received notification of a proposed concentration pursuant to Article 4 of the Merger Regulation by which Synopsys, Inc. ("Synopsys", United States of America) will acquire, within the meaning of Article 3(1)(b) of the Merger Regulation, sole control over ANSYS, Inc. ("Ansys", United States of America) (the "Transaction").[3] Synopsys is designated hereinafter as the "Notifying Party", and Synopsys and Ansys are together referred to as the "Parties", while the undertaking resulting from the Transaction is referred to as the "Merged Entity".[4]

1 OJ L 24, 29.1.2004, p. 1 (the "**Merger Regulation**"). With effect from 1 December 2009, the Treaty on the Functioning of the European Union ("**TFEU**") has introduced certain changes, such as the replacement of "Community" by "Union" and "common market" by "internal market". The terminology of the TFEU will be used throughout this decision.

2 OJ L 1, 3.1.1994, p. 3 (the "**EEA Agreement**").

3 OJ C, C/2024/6996, 19.11.2024.

4 The present Commission decision pursuant to Article 6(1)(b) in conjunction with Article 6(2) of the Merger Regulation and Article 57 of the Agreement on the European Economic Area will be referred to as the "Decision".

1. THE PARTIES AND THE OPERATION

(2) Synopsys offers electronic design automation ("EDA") software, services, and hardware used to design semiconductor devices, such as integrated circuits ("ICs", commonly known as "chips"). EDA tools allow chip designers to plan, design, and verify chips before they are sent to foundries for manufacturing. Additionally, Synopsys offers intellectual property products in the form of pre-designed building blocks of a chip design for implementation in semiconductor devices ("design IP"). In October 2024, Synopsys finalised the sale of its software integrity activities, a third business segment, to Clearlake Capital Group and Francisco Partners.[5] In its most recent financial year (ending 31 October 2023), Synopsys had USD 5.8 billion revenue worldwide (including USD 525 million for its subsequently divested software integrity activities). Of these revenues, [5-10]% are generated in the EEA (USD […]).

(3) Ansys essentially offers multiphysics simulation and analysis ("S&A") software and services to simulate and analyse the behaviour of a product, process, and/or system via digital models. S&A tools are used across a range of industries including automotive, aerospace, industrial machinery, high-tech (including semiconductors), energy, materials and chemicals, consumer products, and healthcare. Further, Ansys also offers EDA tools as well as S&A tools that are exclusively used by chip designers in their chip design workflows and can therefore be considered EDA tools. Ansys' sales of tools used to design chips account for about [20-30]% of its total revenue. In 2023, Ansys had USD 2.3 billion revenue worldwide. Of these revenues, [20-30]% are generated in the EEA (USD […]).

(4) The operation consists in the acquisition of sole control by Synopsys over Ansys, pursuant to a merger agreement dated 15 January 2024, according to which Synopsys will acquire all of the outstanding shares of common stock of Ansys. Therefore, the Transaction constitutes a concentration within the meaning of Article 3(1)(b) of the Merger Regulation.

1.1. The Transaction rationale

(5) The Transaction builds on an existing partnership between Synopsys and Ansys that started in 2017 and was expanded over the course of the following years to offer complementary products to customers designing chips. The Transaction will allow for a deeper integration, also referred to as "native integration" (see paragraph 520 below), of Synopsys' and Ansys' capabilities since the Parties will be able to develop solutions at the source-code level, which would not have been possible under their partnership agreements as independent companies would not disclose their underlying source code due to the risk of IP expropriation.[6]

(6) The Notifying Party states that the Transaction combines two highly complementary businesses in direct response to customer demand for better integration of electronics design and physical simulation and analysis and is driven

[5] Source: Clearlake and Francisco Partners complete acquisition of Black Duck software, formerly known as Synopys Software Integrity Group; accessed on 6 January 2025 at https://clearlake.com/clearlake-and-francisco-partners-complete-acquisition-of-black-duck-software-formerly-known-as-synopsys-software-integrity-group/

[6] Form CO, para. 6 and paras. 548-567.

by two market trends: (a) increased adoption of multi-die chips (as explained at paragraph 51 below) and (b) shift to silicon-to-systems design paradigm (as explained at paragraph 8 below).[7]

(7) The Notifying Party explains that due to their complex architecture, the design of multi-die packages requires tools that enable earlier and more intensive physics analysis in the design flow.[8] In this respect, the Notifying Party submits that, by combining the Parties' capabilities, the Transaction will allow the Parties to develop more comprehensive and seamless design solutions than was the case under their current partnership.[9]

(8) By the shift to the silicon-to-systems design paradigm, the Notifying Party in essence refers to chips, software, and hardware of an electronic system being designed together instead of separately, leveraging virtual models of the chip.[10] The silicon-to-systems design paradigm allows the creation of high-fidelity virtual models of the full physical product (i.e., a "digital twin" including the electronics, electrical and mechanical components) and its changing environment conditions to enable comprehensive virtual testing through simulation.[11]

(9) According to the Notifying Party, these two trends are driving the need for deeper integration of EDA and S&A software to meet the requirements of customers designing increasingly complex and smart systems. Combining Synopsys' EDA technology with Ansys' complementary S&A capabilities will enable more comprehensive, holistic, and seamless design solutions to meet the needs of engineers in the semiconductor industry as well as other industries whose products are becoming increasingly defined by electronics and software.[12]

(10) Finally, the Notifying Party submits that the Transaction will allow the Merged Entity to compete more effectively with rivals already combining EDA and S&A capabilities, such as Cadence and Siemens.[13]

2. UNION DIMENSION

(11) The undertakings concerned have a combined aggregate world-wide turnover of more than EUR 5 000 million (Synopsys: EUR 5 403 million, Ansys: EUR 2 099 million)[14]. Each of them has a Union-wide turnover in excess of EUR 250 million (Synopsys: EUR […], Ansys: EUR […]), but each does not achieve more than two-thirds of its aggregate Union-wide turnover within one and the same Member State. The notified operation therefore has a Union dimension.

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7 Form CO, paras. 24 and 49.
8 Form CO, paras. 55-59.
9 Form CO, paras. 55-59.
10 Form CO, paras. 62-67.
11 Form CO, para. 68.
12 Form CO, para. 72.
13 Form CO, paras. 24 and 76.
14 Turnover calculated in accordance with Article 5(1) of the Merger Regulation and the Commission Consolidated Jurisdictional Notice (OJ C95, 16.4.2008, p. 1).

3. INDUSTRY OVERVIEW

(12) This Section provides an overview of all groups of products that are relevant for the purpose of assessing the Transaction in order to provide context for the relevant market definition and the competitive assessment undertaken in Section 4 and Section 5: optics and photonics software (Section 3.1); EDA (Section 3.3); S&A (Section 3.3); Design IP (Section 3.4). This section will also introduce the main feature of the EDA markets, namely interoperability (Section 3.5), and the main market trends in the EDA markets which is the growth of multi-die chips (Section 3.6).

3.1. Optics and photonics software

(13) Light behaves in different ways when interacting with different materials. It can be reflected, refracted (bent), diffracted (spread around obstacles), and absorbed. Optical and photonic systems are sets of components that exploit these properties of light to perform particular functions.[15]

(14) Optics software are used to simulate the ways in which light behaves in large macro-scale systems involving lenses, mirrors, and prisms in which the system is large enough to allow for light to be modelled as a simple linear ray (also known as ray-tracing).[16] Applications for optics software include (i) displays, such as screens used in smartphones, televisions and computer monitors; (ii) automotive, such as adaptive lighting systems, head-up displays, headlights and rear-view mirrors; (iii) imaging systems, such as camera lenses, optical telescopes and endoscopes for medical imaging; and, (iv) illumination, for projectors and architectural lighting.[17]

(15) Photonics software are used to simulate the ways in which light behaves in smaller nano-scale optical systems and devices which are smaller than the wavelength of light. Accordingly, engineers need to account for the fact that light behaves like a wave and use complex mathematical equations to model the lights' behaviour.[18] Applications for photonics software include (i) complementary metal oxide semiconductor sensors,[19] used in digital cameras, smartphone cameras, scanners and astronomical telescopes; (ii) solar panels; (iii) fibre optics technologies; and, (iv) light detection and ranging technology, a method used in self-driving vehicles, mapping and surveying to measure distances and map surroundings.[20]

3.2. EDA

(16) In the present decision, EDA is understood as referring to software tools and services used to design and verify chips before they are sent to chip manufacturing plants (known as "foundries") for production.

(17) Chips are small electronic devices made up of several interconnected electronic components. A chip is protected by a protective enclosure, also known as package, that is typically made of plastic, metal, or ceramic. The package protects the chip

15 Form CO, para. 857.
16 Form CO, para. 859.
17 Form CO, para. 861.
18 Form CO, para. 860.
19 A complementary metal oxide semiconductor sensor is a semiconductor device comprised of transistors and photodiodes to capture light and convert it into electrical signals.
20 Form CO, para. 862.

from corrosion and physical damage and creates electrical connections between the chip and the printed circuit boards ("PCB")[21] onto which the chips are mounted after manufacturing. Most electronic systems – such as phones or cars – use several types of chips, and PCBs can be used to connect and integrate them.[22]

(18) Based on the type of calculations they perform, chips broadly fall into three categories, which reflects their respective use cases:

(a) **Analog chips** measure and process continuous analog data that comes from real-world signals such as speed, temperature, and electrical current. Analog chips can be used in a wide range of applications, including amplifiers, filters, oscillators, voltage regulators, and power management circuits. They are commonly found in electronic devices such as audio equipment, radio frequency transceivers, communications, sensors, and medical instruments.

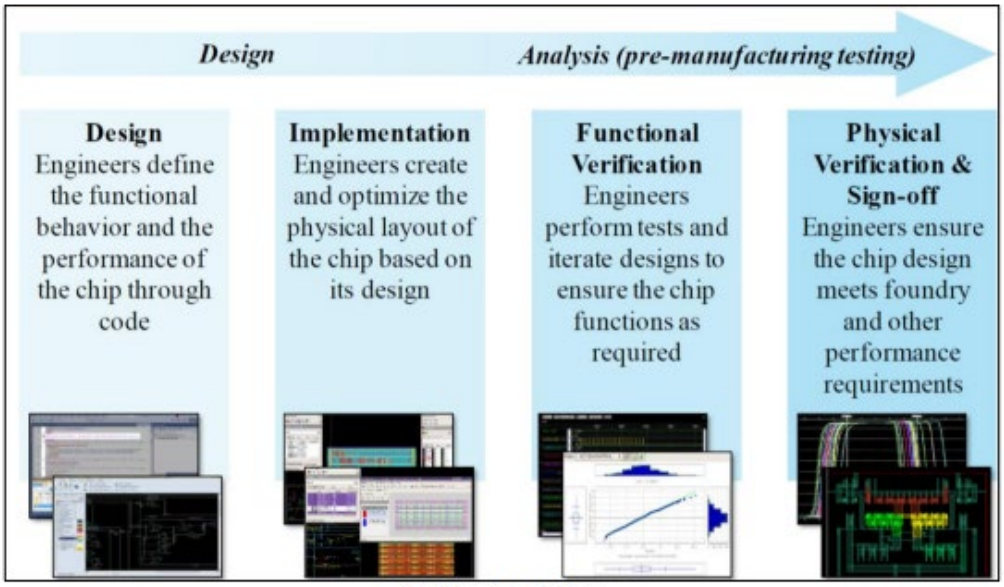
(b) **Digital chips**, in contrast to analog chips, process digital signals (i.e., binary information). Digital chips can be used for memory, storing data, or logic. They are used in computers (e.g., for central processing units ("CPUs"), microprocessors or microcontrollers ("MPUs" or "MCUs"), digital signal processors ("DSPs"), graphics processing units ("GPUs") and a variety of other digital applications.

(c) **Mixed-signal chips** include both analog circuits and digital circuits on a single semiconductor wafer (see below for more details). They are traditionally used to convert digital signals to analog signals, and vice versa. For example, the chip in a pair of headphones receives a digital signal (e.g., from a mobile phone), and emits an analog signal (a sound wave) through the speaker. In recent years, as chips become more complex and perform more sophisticated functions, they often involve both digital and analog functions. For example, a computer microprocessor is primarily a digital chip operating on logic functions and binary data, but it also has a small analog component that enables interfaces with the real world (e.g., networking devices such as Ethernet).[23]

(19) Chip design requires a number of different processes ("design flows") and tools before the chip can be manufactured. As illustrated below, a chip design flow typically consists of the following stages: design (defining what the chip will do), implementation (creating and optimizing the physical layout of the chip), functional verification (ensuring that the chip functions according to the intended design), physical verification (testing the chip's layout design) and sign-off (testing compliance with foundry requirements and regulations).

21 Form CO, para. 573.
22 Form CO, para. 190.
23 Form CO, para. 180.

Figure 1: Chip design flow[24]



Source: the Parties

(20) These chip design stages are largely similar for all chips. However, there are slight variations in the design flow depending on the type of chip (analog, digital and/or mixed signal), as illustrated below.

Figure 2: Analog chip design flow



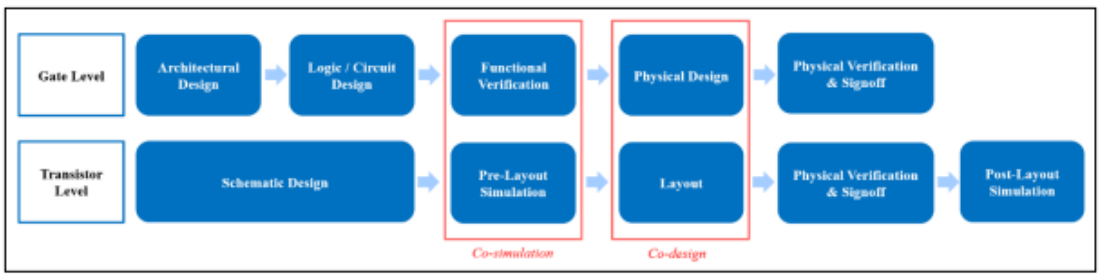
Source: the Parties

Figure 3: Digital chip design flow



Source: the Parties

Figure 4: Mixed signal chip design flow



Source: the Parties

[24] Form CO, page 64.

(21) For each step in the chip design process, EDA companies offer a range of tools with various functionalities. The EDA tools required in a chip design flow depend on the type and complexity of the chip.

(22) A typical chip design flow will involve between five and twenty EDA tools across the various design stages, typically from various EDA companies since customers routinely 'mix-and-match' tools with different functionalities from different providers across their design flows. Those customers thereby rely on the interoperability between the different vendors' EDA tools[25], as will be explained in more detail below at Section 3.5.

(23) Customers 'mix-and-match' EDA tools from different providers for a number of reasons, and in particular because (i) they want to use the tools they consider best in terms of quality and performance at each step in the design flow (a so-called 'best of breed' approach), (ii) no single EDA vendor can offer customers all the tools they want and/or need across all steps in the design flow, and/or (iii) their teams are already used to working with a given tool and there is a cost to switching tools, for example training employees to use a new tool or building a new design flow.[26] Also, customers typically do not swap tools in a particular design flow after a project has begun.[27]

(24) Further, certain customers, particularly large ones, license more than one tool with the same functionality, for various reasons, including the fact that a given tool may perform better or less well depending on the chip being designed, to mitigate technology risk or to strengthen their negotiation position vis-à-vis providers.

(25) The EDA sector is concentrated around three players: Synopsys, Cadence, and Siemens, which all offer a broad portfolio of tools covering a large number of design steps.[28]

(26) Cadence is a multinational corporation offering a broad suite of EDA tools for designing chips and other electronic devices such as PCBs. Cadence has EDA tools in all stages of the digital and analog chip design workflow and in all the tool categories required to design a basic digital or analog chip. Cadence also provides a variety of S&A tools.[29] Further, it also provides various design IP products. Cadence had global revenues of USD 4.09 billion in 2023.[30]

(27) Siemens is a multinational corporation that supplies products and services throughout the world, mainly in information and communications, automation and control, power supply, transportation, medical technology, lighting, financial services and real estate,[31] that is active in a variety of industries. Siemens acquired EDA provider Mentor Graphics in 2017[32], which it rebranded as Siemens EDA. Siemens has EDA tools in various stages of the digital and analog chip design workflow and in several of the tool categories required to design a basic digital or

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25 Form CO, para. 17.
26 Form CO, paras. 621, 784-785, 777 and 977-978.
27 Form CO, para. 777.
28 Form CO, paras. 193-194.
29 Form CO, para. 194.
30 Source: Cadence press release of 12 February 2024, entitled "Cadence Reports Fourth Quarter and Fiscal Year 2023 Financial Results"
31 Commission decision of 30 April 2003 in case M.2861- *Siemens/Drägerwerk/JV*, para. 5.
32 Commission decision of 27 February 2017 in case M.8315 - *Siemens/Mentor Graphics*.

analog chip. Siemens also has a significant S&A business.[33] Its Digital Industries segment, which *inter alia* contains Siemens' EDA and S&A software portfolio, had revenues of over € 21.9 bn in 2023, of which 23% was achieved through the sale of software.[34]

(28) Among the remaining EDA providers, Ansys focuses on EDA tools used at the physical verification and sign-off stages. That said, Ansys also offers EDA tools that are used earlier in the design flow.[35]

(29) Other EDA providers offer tools for certain capabilities or stages in the chip design process (sometimes described as "point" tools).[36] These include companies such as Altair, Dassault, Keysight, Lorentz, MathWorks and Zuken.

(30) The main EDA customers are semiconductor companies, systems companies, and foundries.[37] Semiconductor companies design chips for sales to customers, which are typically large enterprises. Examples of semiconductor companies include Intel, Samsung Electronics, Qualcomm, Broadcom, NVIDIA, SK Hynix, AMD, ST Microelectronics, Texas Instruments, among others. System companies also design chips, but for use in their own products. For example, Apple designs its own processors to power its mobile devices and computers. Alphabet, Amazon, Meta, and Microsoft all design their own chips to accelerate AI-workloads in their cloud datacenters. In addition to tech companies, systems companies include those active in a range of other activities such as automotive, aerospace, and industrial equipment sectors. Foundries manufacture chips based on designs provided by chip designers, who can be semiconductor or system companies. Examples include TSMC, Samsung Foundry, Intel Foundry Services, Global Foundries, UMC, SMIC and Tower Semiconductor.[38]

(31) In 2023, the sales of EDA tools amounted to USD 11.091 billion globally. Synopsys predicts that the EDA sector will grow by a [10-20]% compound annual growth rate ('CAGR') between 2023 and 2028.[39]

3.3. S & A

(32) S&A tools enable engineers to simulate and analyse the behaviour of a product, system, or process via digital models. By using digital modelling and simulations, engineers can perform "what-if" analyses, evaluate alternative designs, and explore how their products will react to different situations.[40]

(33) Through these processes, designers test the durability, safety, and reliability of a product by digitally simulating real-world scenarios. These may involve general physics-based calculations, but also more targeted tools aimed at simulating specific scenarios, such as structural, fatigue, thermal, optical, acoustics, and

33 Form CO, para. 194.
34 Siemens – Business Fact Sheets; accessed on 17 December 2024 at https://assets.new.siemens.com/siemens/assets/api/uuid:f3dbe372-808e-40de-b980-0926f16c343d/Siemens-Business-Fact-Sheets.pdf
35 Form CO, paras. 13-14.
36 Form CO, paras. 195-196.
37 Form CO, para. 198.
38 Form CO, para. 198.
39 Form CO, para. 772 and footnote 1005.
40 Form CO, para. 242.

computational fluid dynamics issues. S&A therefore provides virtual modelling and analysis of initial product concepts, without the need for physical prototypes.[41]

(34) S&A tools are used across a range of industries including automotive, aerospace, industrial machinery, high-tech, energy, materials and chemicals, consumer products, and healthcare. For example, S&A tools allow car manufacturers to simulate crash testing (rather than actually crashing a prototype), test the effect of physical phenomena such as wind or water on their product designs (rather than, for example, testing the product in a physical wind tunnel), and simulate the effect of light on virtual prototypes.[42]

(35) Advanced S&A tools enable the creation of a "digital twin" virtualizing the physical aspects of the relevant product, which is cheaper and easier than physically testing it.

(36) Certain S&A software is designed for semiconductor applications to simulate the physical characteristics of a chip. For example, there are S&A tools that allow chip designers to simulate how a chip design will function with respect to heat, electromagnetic signals, or power. [43] Hereafter, S&A tools used in the chip design process will be referred to as EDA tools.

3.4. Design IP

(37) Companies designing chips need to develop or procure both design IP and EDA tools.[44]

(38) Design IP, also known as semiconductor or silicon IP, refers to predesigned blocks which perform a specific function within a chip, for instance memory access. Such blocks can be developed in-house or licensed to multiple customers for use as building blocks in different chip designs.[45]

(39) Within design IP a distinction may be made between processor design IP (i.e., IP for the design specifically of the central processing unit ('CPU'), digital signal processor ('DSP'), graphics processing unit ('GPU'), image signal processor ('ISP'), and neural processing unit ('NPU')) and non-processor design IP (e.g., IP for memory controllers, interface protocols, analog and digital IP blocks, optimised functions, and subsystems that collectively enable the functionality, connectivity, and performance of the semiconductor chip).

(40) Synopsys competes to a limited extent in processor IP. It mainly develops and licenses non-processor design IP, notably foundation IP, interface IP and other IP.

(41) Foundation IP (also known as 'physical IP') constitutes the next level of building block for the chip design above the transistor level. It broadly consists of the following categories: (i) embedded memories (also referred to as "memory compilers" because of how they are created), (ii) non-volatile memories/other memories, and (iii) physical libraries (also known as standard cell libraries or logic

41 Form CO, para. 243.
42 Form CO, para. 244.
43 Form CO, para. 246.
44 Form CO, Appendix 1 – Intellectual property business – para. 40.
45 Form CO, Appendix 1 – Intellectual property business – paras. 2, 4 and 18.

libraries), that is a collection of well-defined and pre-characterised logic cells used in digital design.

(42) Interface IP products enable communication between different components within a chip or between chips through industry standard interfaces such as UCIe, USB, PCIe, Ethernet, HDMI and Bluetooth Low Energy. Wired interface IP products ensure support for various wired interface standards, while wireless interface IP products ensure support for different wireless standards. Wired and wireless interface IP contain both a PHY (= hard IP) and a controller (= soft IP) portion[46].

(43) Other IP is a "catch-all" category encompassing a range of design IP products, beyond those mentioned above. Within that category, a further segmentation can be made between security IP and miscellaneous other types of IP. Security IP products enable various security functionalities and features to be incorporated into SoC designs.

(44) Design IP can generally be categorised as either soft IP or hard IP, and sometimes as both.[47]

(45) Soft IP blocks are generally offered as synthesizable RTL models, and also sometimes as generic gate-level netlists. Soft IP blocks enter the EDA design flows at the design stage. Conceptually, soft IP is subsequently converted into hard IP through processing by RTL synthesis tools, design-for-test / test IP tools, place & route tools, and timing analysis tools.[48]

(46) Hard IP blocks are offered as layout designs and can be directly dropped by a consumer to the final layout of the chip. Unlike soft IP, these blocks cannot be customised by the customer. Physical verification and sign-off tools can be run directly on the hard IP blocks.[49]

(47) Besides Synopsys, companies active in design IP include Arm, Alphawave, Aragio, Cadence, M31, Rambus and Verisilicon.[50]

3.5. Interoperability

(48) Different EDA software tools interoperate during the chip design as the output data from one EDA tool are read by another, and one tool calls on certain functions or data of another tool. Interoperability ensures that each tool works with an adjacent tool in the design flow, irrespective of the EDA provider. Interoperability between EDA tools is a standard business practice in the EDA industry.[51]

(49) There are different ways in which EDA vendors ensure interoperability between EDA tools. Interoperability is achieved primarily through industry standard languages and file formats ("baseline" interoperability). Further, EDA vendors may

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46 'PHY' refers to 'physical layer', which is an abstraction layer that transmits and receives data. The PHY part encodes data for transmission and decodes data with a specific modulation speed of operation, transmission media type, and supported link length. The 'controller' part is synthesizable soft IP that implements a complete logical implementation of a given protocol (e.g., USB, Ethernet).

47 Form CO, Appendix 1 – Intellectual property business – para. 6.

48 Form CO, Appendix 1 – Intellectual property business – para. 4.

49 Form CO, Appendix 1 – Intellectual property business – para. 4.

50 Form CO, Appendix 1 – Intellectual property business – para. 36.

51 Form CO, para. 17.

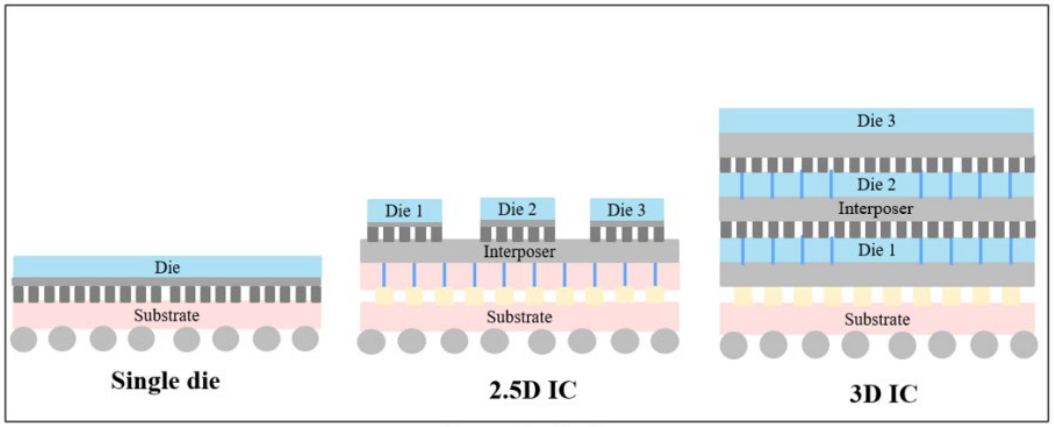
conclude interoperability agreements for developing proprietary file formats and/or application programming interfaces ("APIs") for their tools to interoperate.[52] Finally, where a vendor has different EDA tools that serve adjacent functions in the design flow, he may decide to natively integrate its tools. In the latter case, the functionalities are delivered through one single EDA tool. However, even in such case the vendor will generally continue to sell the various tools that have been integrated into a single solution as standalone tools.[53]

(50) Each type of interoperability will be described in more detail at Section 5.4.3.1.1. below.

3.6. The growth of multi-die chips

(51) Today's most advanced chips, particularly those used for high-performance computing ('HPC') and artificial intelligence ('AI') training and workloads, are based on multi-die architectures. Instead of a single monolithic chip, multi-die design involves assembling different pieces of a chip (known as "dies" or "chiplets") in a sophisticated package and connecting them together to optimise performance.[54] This includes both incorporating dies placed next to each other on the same surface (substrate) but separated by an interposer (known as 2.5D architecture) or stacking dies on top of each other, separated by interposers (known as 3D architecture), as illustrated below.

Figure 5: single die vs. multi-die[55]



Source: the Parties

(52) Multi-die designs offer several potential advantages. First, large and complex chip designs can be partitioned into smaller dies that are proven, resulting in higher manufacturing yields and lower silicon costs over time. Second, the different dies can be manufactured independently, potentially using different process nodes to manage costs. Third, assembling dies in multi-die packages can enable a chip to exceed the size limit of 2D designs and deliver higher performance. Fourth, multi-die designs are modular and enable designers to customize products to different customer needs and applications by mix-and-matching separate dies.[56]

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52 Form CO, paras. 230-232.
53 Form CO, paras. 1092-1094.
54 Form CO, para. 51.
55 Form CO, para. 188.
56 Form CO, para. 52.

(53) Companies offering multi-die chips today include Intel, AMD, and Nvidia. Some system companies like Amazon also already design their own HPC chips with multi-die architectures. Multi-die chip designs are used across a variety of applications such as server, personal computer ('PC'), consumer systems, and automotive.[57]

(54) The complex architecture of multi-die chips raises new and/or more complex physical issues that need to be solved such as heat dissipation, warping, and cracking of packages due to mechanical stress. This requires tools that enable earlier and more intensive physics analysis in the design flow.[58]

(55) Multi-die chips are expected to constitute a market of USD [0-200] by 2027 and more than USD [100-300] by 2032.[59] The growth in sales of EDA tools will be particularly impacted by the demand for multi-die chips. Synopsys expects that by 2029, EDA tools used for multi-die chips will account for ~33% of sales of all EDA tools, and that the CAGR for EDA tools for multi-die will be + 40% over the period 2023-2029; compared to + 7% for the remaining EDA tools.[60]

4. RELEVANT MARKETS

4.1. Optics and photonics software

4.1.1. Product market definition

4.1.1.1. Past Commission decisions

(56) The Commission has not previously defined a market for optics and/or photonics software.

4.1.1.2. The Notifying Party's views

(57) The Notifying Party finds it appropriate to distinguish optics software from photonics software since they serve distinct purposes and are not interchangeable.[61] From a demand-side perspective, these software tools do not have the same use cases, and customers require both types of software to fully design an optical structure.[62] Further, from a supply-side perspective, the Notifying Party submits that companies typically specialize in either optics software or photonics software due to photonics software requiring specialised expertise in wave-based light modelling.[63]

(58) With respect to both optics and photonics software, the Notifying Party submits that it would not be appropriate to further segment the market for the supply of optics software and/or the market for photonics software (i) between design and simulation, (ii) by functions/use-cases and/or (iii) by industry sector.[64]

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57 Form CO, para. 53.
58 Form CO, para. 55.
59 Form CO, para. 53 and Annex PN RFI 1 Q22 (Yole Report, 2022, p. 19).
60 Form CO, Annex M.11481 - 4(c)-10 […], slide 18.
61 Form CO, para. 889.
62 Form CO, paras. 889-891.
63 Form CO, para. 892.
64 Form CO, paras. 894 and 910.

4.1.1.3. Commission's assessment

(59) The Commission's market investigation tested whether there is a separate market for the supply of optics software and the supply of photonics software.

(60) The results of the market investigation,[65] as well as evidence submitted by the Parties,[66] confirm that optics software and photonics software serve distinct purposes and are not substitutable. Further, the results of the market investigation did not suggest alternative product market definitions.

(61) In light of the above, for the purposes of this Decision, the Commission concludes that there is a separate market for the supply of optics software, distinct from the market for the supply of photonics software.[67]

4.1.2. Geographic market definition

4.1.2.1. Past Commission decisions

(62) The Commission has not previously defined a market for optics and/or photonics software.

4.1.2.2. The Notifying Party's views

(63) The Notifying Party submits that the geographic scope of the market for the supply of optics software and the market for the supply of photonics software is global.[68]

4.1.2.3. Commission's assessment

(64) The results of the market investigation,[69] as well as evidence submitted by the Parties[70], confirms that the market for the supply of optics software, and the market for the supply of photonics software, are global in scope.

(65) In light of the above, for the purposes of this Decision, the Commission concludes that the geographic scope of the market for the supply of optics software and the market for the supply of photonics software, is worldwide.

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65 Questionnaire to users and providers of optics and photonics software, questions C.A.1. and C.A.2.

66 Form CO, paras. 884-893.

67 The Parties' combined market shares on the market for the supply of optics software and on the market for the supply of photonics software are presented in section 5.2 below. There is no evidence in the Commission's case file that the competitive dynamics in any of the plausible segmentations would be materially different and/or lead to different conclusions from the effects that the Transaction is likely to have on the market for the supply of optics software and the market for the supply of photonics software. For the purposes of this Decision and given the divestment of Synopsys' entire optics and photonics businesses, the question as to whether the market for the supply of optics software and the market for the supply of photonics software should be further segmented between design and simulation, by functions or use-cases, or by industry sector can be left open, as it does not have an impact on the competitive assessment of the Transaction.

68 Form CO, paras. 920-926.

69 Questionnaire to users and providers of optics and photonics software, questions C.B.1. and C.B.2.

70 Form CO, paras. 920-926.

4.2. EDA

4.2.1. Product market definition

4.2.1.1. Past Commission decisions

(66) The Commission has previously considered a separate market for the supply of EDA tools as part of the larger market for product lifecycle management ("PLM") in M.8315 - *Siemens/Mentor Graphics*, but ultimately left the market definition open. In that decision, the Commission also considered whether it was appropriate to further segment EDA tools by their end use resulting in segments for (i) Printed Circuit Boards ("PCBs"), (ii) integrated circuits ("ICs"), and (iii) Computer-Aided Engineering ("CAE"), but ultimately left the market definition open.

4.2.1.2. The Notifying Party's views

(67) The Notifying Party submits that an overall market for EDA tools would be too broad to constitute a single product market.[71] Competition between EDA tools should be assessed at the **functional level** of the tool, which is the most granular plausible segmentation, given that EDA tools offer different functions, which are generally not substitutable from a demand side perspective.[72] In addition, from the supply side, there is limited substitutability as the development of EDA tools requires not only general expertise in software development, mathematics, and electronics, but also skills that are specific to a certain subset of tools.[73]

(68) The Notifying Party does not consider it appropriate to further segment EDA functions according to (i) the type of semiconductor device (with the exception of EDA tools for ICs and PCBs/CAE), (ii) the stage of the semiconductor design flow, or (iii) industry sector.[74]

(69) As regards the potential segmentation of EDA functions based on **type of semiconductor device**, the Notifying Party maintains that EDA tools may be used for one or several different types of semiconductor devices. At a high level, EDA tools provide functions for digital chip design, analog chip design, or both types of designs. The design of mixed-signal chips (which have both digital and analog components) requires digital and analog tools, as well as specialised tools for mixed-signal designs that enable more efficient exchanges of information between digital and analog components. The design of multi-die chips (which are comprised of different chiplets) may require, for example digital, analog or mixed-signal chip design tools.[75] The design of photonic chips may involve specialised tools for photonic chip designs as well as EDA tools used for analog chips.[76]

(70) While the Notifying Party considers that a segmentation according to the type of chip is not appropriate due to overlapping functionalities, the Notifying Party considers that EDA tools for the design of ICs would be distinct from EDA tools for the design of PCBs and CAE: EDA tools for ICs are used to design chips (such as digital, analog chips, as described above), whereas EDA tools for PCBs are used

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71 Form CO, para 301.
72 Form CO, paras. 301-303 and 306-307.
73 Form CO, para 308.
74 Form CO, paras. 314-319.
75 Form CO, para 315.
76 Form CO, para 498-501, 507; Synopsys, […], 4 December 2024.

to design motherboards, and CAE tools concern software used by manufacturers to analyse and test the functionality of the finished PCB, incorporating any relevant ICs.[77]

(71) As regards the potential segmentation of EDA functions based on the stage of the semiconductor design flow, the Notifying Party submits that different EDA tools are used for each **stage of the design flow** and that, in general, EDA tools for a particular stage are not substitutable for those used in another stage. However, certain tools could be used at several different stages.[78]

(72) Finally, as regards the potential segmentation of EDA functions based on the industry sector, the Notifying Party maintains that it would be the type of semiconductor device required, not the **industry** (e.g. semiconductor companies or automotive companies designing their own chips) that dictates a customers' choice of EDA tool. For example, tools for analog chips design would be used across different industries for different end uses (e.g. for use in a car or use in a mobile phone). This would not be changed by the fact that certain industries might focus on the design of different chips (e.g. with semiconductor companies focusing on the design of digital chips).[79]

4.2.1.3. Commission's assessment

(73) For the reasons explained below, the Commission concludes that segmenting EDA tools **at the functional level**, i.e. by each EDA function of a tool, is the most appropriate way to define the relevant product market for the purpose of this Decision.

(74) **First**, the Commission notes that while in M.8315 - *Siemens/Mentor Graphics* the Commission considered a wider market definition, the market definition was ultimately left open, as noted in the Commission's Market Definition Notice, market definition is based on the facts of the case. Where past Commission decisions concerning a specific market exist, the Commission may start its analysis from such prior decision and verify whether the definition of the relevant market used in those past decisions may be applied to the case at hand. However, the Commission is not bound to apply the definition of a relevant market from its past decisions in future cases.[80]

(75) To reflect the most recent market developments in the EDA markets (see Section 3 above) and identify the most appropriate product market definition for the purposes of this Decision, the Commission undertook an extensive product mapping exercise. The Commission engaged with the Parties and their main competitors to comprehensively map the Parties' and their competitors' products, as well as the different EDA segments in which these products compete with one another.[81]

(76) **Second**, the Commission's product mapping exercise confirmed that competition between EDA tools primarily occurs at the functional level, i.e. based on the tool's

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77 Form CO, para. 303, 313.

78 Form CO, para 314.

79 Form CO, para 318.

80 Commission Notice on the definition of the relevant market for the purposes of Union competition law (referred to as "Market Definition Notice"), para. 14.

81 Subsequently, the Commission requested revenue and market shares based on the Parties' best estimates. See Annex A.

functionality. For example, a "gate-level power integrity analysis" tool performs voltage drop and electromigration (EM/IR) analysis to check a chip's reliability when using power.

(77) As explained further in Annex A, which forms an integral part of this Decision, as part of the product mapping exercise, the Parties and their main competitors identified all functionalities of the Parties' and their competitors' products and allocated them to the four categories described below. The four categories described below served as a framework for identifying all possible segmentations for any given EDA tool.

(a) **Design flow (Level 0 – L0):** Reflects the type of IC and semiconductor device for the design of which an EDA tool is used: (i) Digital Design Flow, (ii) Analog Design Flow, (iii) Mixed-signal Design Flow, (iv) Photonic Design Flow, (v) Multi-die chip Design Flow, (vi) PCB Design Flow, (vii) Packaging Design Flow.

(b) **Presentation (Level 1 – L1):** This category includes the "front-end" and "back-end" of the design flow.[82] However, these terms are not used by all market participants.

(c) **Design stage (Level 2 – L2):** This sub-category includes the different stages of the design flow. Earlier stages generally concern the design of a chip, while later stages concern the verification. For illustration, the Digital Design Flow (Annex A, Table 2) front-end includes the stages "*Architectural Design*", i.e. a high level logical design of the chip, "*Logic/Circuit Design*", a more detailed logical design of the chip and "*Functional Verification*" that ensures that the logical design is correct. The back-end includes the stages "*Physical Design*", i.e. the translation of the logical design into the physical design of a silicon die and "*Physical Verification & Sign-off*" that ensures the physical design works as intended.

(d) **Function (Level 3 – L3):** This category includes the specific functions of EDA tools within each design stage. For example, "*Gate-level Power Integrity Analysis*" is an EDA function in the "*Physical Verification & Sign-off*" stage of the Digital Design Flow. This is considered the **level 3 (L3)** of the design flow.

(78) On this basis, the product mapping exercise identified **59 unique "EDA functions"**[83] (Level 3 category), (indexed by a unique "*Functional ID*", in the following "**functional level**"). This segmentation reflects all possible EDA functions, irrespective of whether the same EDA function appears in more than one design flow and/or design stage.[84] Namely, the product mapping exercise showed

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82 The front-end concerns the logical design of a chip, while the back-end concerns the translation of this conceptual design into a physical design of the chip on a silicon die.

83 The Functional ID is defined as the minimum of Segment IDs (see next sentence) with the same function. For example, "Circuit Simulation" appears twice in the Analog Flow and twice in the Multi-die Flow in stages Pre-Layout Simulation and Post-Layout Simulation, Segment IDs 33, 50, 58 and 77, and therefore is assigned Functional ID 33. The Commission also notes that some of these EDA functions appear in more than one design flow (Level 0) and/or more than one design stage (level 2). This yields a total of **88 design flow combinations** indexed by a unique "*Segment ID*" (in the following "**segment level**" or "**Segment ID level**").

84 EDA functions are defined broadly, including the photonic design flow, PCB and packaging design and EDA tools outside design flows. In addition, the product mapping also includes Design IP. There

that most EDA functions are specific to only one design flow (Level 0) and/or only one design stage (Level 2). For example, "*Gate-level Power Integrity Analysis*" is an EDA tool function exclusively present in the "*Digital Design Flow"*.[85] A lesser proportion of EDA functions appear in more than one design flow (Level 0) and/or more than one design stage (Level 2).[86]

(79) **Third**, the results of the market investigation confirmed that EDA tools with different functions are not substitutable from a demand-side perspective.

(80) In the first place, several internal documents from the Parties compare their tools with those of their competitors at the functional level.[87] For example, some documents map out competitors' tools, their functionality and the alternative that Synopsys and/or Ansys offers.[88] The Parties' main EDA competitors, Siemens and Cadence, also consider that EDA tools compete at the functional level.[89]

(81) In the second place, the results of the market investigation confirmed that EDA tools with different functionalities are generally not considered to be substitutes by customers, who choose their EDA tools based on the functionality they need for a given chip design project.[90]

(82) In the third place, the Commission notes that the concerns raised by some market participants with respect to horizontal or conglomerate effects of the Transaction focused on the specific functions of EDA tools (e.g. gate-level power integrity analysis, RTL power consumption analysis, etc.), where the market participants feared the anticompetitive effects could arise.[91] Their submissions therefore further indicate that market participants primarily compete for the demand at the level of specific EDA functions, rather than at broader levels (e.g. a design stage level or EDA overall).

(83) **Fourth**, the results of the market investigation confirmed that EDA tools with different functions are not substitutable from a supply-side perspective. The necessary conditions for the market to be broadened based on supply substitution are (i) that most, if not all, suppliers are able to switch production between products in the range of related products and have the incentive to do so when relative prices or demand conditions change; (ii) that suppliers incur only insignificant additional sunk costs or risks when they switch production; and (iii) that they can offer all

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are 9 Design IP segments. Including Design IP, there is a total of 68 Functional IDs and 97 Segment IDs.

85 Power integrity analysis checks a chip's reliability when using power, to ensure it will continue to function correctly. This includes checking that the chip will not succumb to electromigration ("*EM*"), where electric current changes a conductor's structure, or a drop in voltage ("*IR*").

86 For example, Circuit Simulation appears both in the Analog Design flow and in the Multi-die chip Design Flow. In both flows, it appears in the Pre-Layout Simulation and Post-Layout Simulation design stages.

87 Form CO, Ansys internal documents Annex 5.4(c)(ANSS) – 007 – […]; Annex 5.4(c)(ANSS) – 009 – […]; Annex 5.4(c)(ANSS) – 022 – […]; Annex 5.4(c)(ANSS) – 024 – […]; and Synopsys internal documents Annex 5.4(c)(SNPS) - 033 - 5 […]; Annex 5.4(c)(SNPS) - 030 - […]; Annex 5.4(c)(SNPS) - 012 - […]

88 Annex 5.4(c)(ANSS) – 022 – […]; Annex 5.4(c)(ANSS) – 024 – […].

89 See inter alia, Market participant's submission of 14 June 2024; and Market participants' reply to the European Commission's RFI 1 and 3.

90 Replies to questionnaire to customers of EDA and design IP, questions D.A.A. to D.A.F.

91 Market participant's submission to the European Commission dated 14 June 2024; Market participant's submission to the CMA dated 12 April 2024.

products in the range effectively in the short term.[92] These conditions are not satisfied, for the reasons set out below.

(84) In the first place, the Commission notes that no EDA vendor offers EDA tools for all functions and the majority of EDA vendors has only a limited offering of EDA tools, performing specific functions.[93] Bigger EDA vendors often increase their product offering via acquisitions rather than native development.[94] In that regard, the Notifying Party also confirms that the majority of its R&D does not concern the development of new EDA tools, but rather the upgrade of its existing EDA tools.[95] Indeed, as the Notifying Party confirms, there is limited substitutability from a supply-side perspective because the development of EDA tools requires not only general expertise in software development, mathematics, and electronics, but also specific skill sets. [96]

(85) In the second place, the development of new EDA tools involves significant R&D costs that cannot be recuperated and are therefore sunk. In addition, the development of new EDA tools involves significant risks, because the outcome of R&D efforts is uncertain and it is unclear whether, upon its development, the new EDA tool will be on par with the best EDA tools on the market at the time of completion.

(86) In the third place, market participants suggest that the development of new EDA tools can take several years.[97]

(87) **Fifth**, the Commission has also considered whether it is appropriate to segment EDA functions according to the **type of design flow** and **design stage**, as some EDA functions are used for more than one type of design flow and/or design stage (e.g. ESD analysis tool can be used in the analog, digital and multi-die design flows; thus, it would be possible to assess whether the relevant market for the ESD analysis tool should be further segmented by type of design flow).

(88) In the first place, the product mapping exercise shows that most EDA tools are used in one specific design flow and/or in one specific design stage. Out of 59 EDA functions, only 22 EDA functions appear in more than one design flow and/or design stage.[98] Likewise, there are no EDA functions used both for IC design flows[99] as well as for the PCB and/or packaging design flows.

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92 Market Definition Notice, para 33.

93 The Parties' product mapping identifies 48 EDA vendors, see Annex A, Section 3.1.

94 Agreed minutes of the conference call of 23 July 2024 with a market participant, para. 4.

95 Form CO, para 824.

96 For example, circuit simulators for analog chips would require knowledge in linear algebra, numerical analysis and device physics, while digital simulators would require knowledge in Boolean algebra, finite state machines and event driven programming. Form CO, paragraph 308.

97 For instance, replies to questionnaire to customers of EDA and design IP, question D.A.C.4.2 and market participant's response to the European Commission's RFI 2, para. 23.2.

98 15 appear in multiple design flows (albeit in the same design stage): 8 in the digital and multi-die flows, 4 in the analog and multi-die flows and 3 in the digital, analog and multi-die flows. Out of the 15, 4 appear in multiple design stages (albeit within the same design flow) and 3 in multiple design flows and multiple stages: 1 in the digital and analog flows, 1 in the digital and multi-die flows and 1 in the analog and multi-die flows.

99 Meaning: (i) Digital Design Flow, (ii) Analog Design Flow, (iii) Mixed-signal Design Flow, (iv) Photonic Design Flow, (v) Multi-die chip Design Flow, (vi) PCB Design Flow, (vii) Packaging Design Flow.

(89) In the second place, the distinction between different design flows is not clear-cut, and appears the least clear for mixed-signal chips and multi-die chips, which combine both digital and analog elements, therefore generally requiring analog and digital EDA tools. Further, the design of photonic chips relies on analog tools as well as specialised tools with functions that are unique to the photonic design flow.[100]

(90) In the third place, in the ordinary course of business, the Parties and their competitors do not track revenues of EDA tools based on the design flows/design stages in which the EDA tools are used.[101]

(91) **Finally,** there are no indications that it would be appropriate to segment EDA tools according to industry.

4.2.1.4. Conclusion

(92) In light of the above, the Commission concludes that, for the purposes of this Decision, EDA markets should be defined at the functional (i.e. tool) level, i.e. by each EDA function (i.e. tool), without further segmenting EDA tools into narrower markets according to the type of design flow and/or design stage and/or industry. For the purposes of the present Decision, the Commission will conduct its competitive assessment in the markets, which correspond to the EDA functions listed in Table 8 of Annex A and which are identified as affected in Section 5.1 below. Further, for the purpose of this Decision, the Commission considers that it is not appropriate to define wider markets, like an overall market for PLM, EDA, or any EDA market sub-segments depending on the use case (IC, PCB or CAE).

4.2.2. Geographic market definition

4.2.2.1. Past Commission decisions

(93) In M.4608 – *Siemens/UGS*, M.5763 – *Dassault Systèmes/IBM DS PLM Software Business* and M.8315 - *Siemens/Mentor Graphics* the Commission has considered a potential worldwide geographic scope for the supply of PLM software but ultimately left the exact market definition open.[102]

4.2.2.2. The Notifying Party's views

(94) The Notifying Party submits that the appropriate geographic market definition for EDA tools for chips is global as the conditions for competition are sufficiently homogenous globally. In particular, EDA vendors offer their solutions globally and do not differentiate their product offering based on geography, EDA customers procure their tools from suppliers situated anywhere in the world, and the main parameters of competition (e.g., quality, price, technical capabilities, performance, contractual terms, customer support, etc) are the same regardless of the country considered.[103]

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100 Form CO, paras. 498-501, 507; Synopsys, […], 4 December 2024.

101 See Annex A, Section 2. Market participant's reply to the European Commission's RFI 1 and 3, market participant's reply to the European Commission's RFI 1 and 3.

102 M.8315 - *Siemens/Mentor Graphics*, paras 36-39 and the precedents cited therein: Commission decision of 29 March 2010 in case M.5763 – *Dassault Systèmes/IBM DS PLM Software Business*, para. 21; and Commission decision of 27 April 2007 in Case M.4608 – *Siemens/UGS*, para. 11.

103 Form CO, para. 321.

4.2.2.3. Commission's assessment

(95) The results of the market investigation confirmed that EDA tools and providers are the same, irrespective of where customers are located, and that contracts are worldwide in scope.[104]

(96) Further, the results of the market investigation did not suggest alternative geographic market definitions.

(97) In light of the above, for the purposes of this Decision, the Commission concludes that the geographic scope of the EDA markets is worldwide.

4.3. Design IP

4.3.1. Product market definition

4.3.1.1. Past Commission decisions

(98) In previous decisions, the Commission has considered a potential market for serializer/deserializer ('SerDes') IP – a type of design IP – and left the exact market definition open.[105]

4.3.1.2. The Notifying Party's views

(99) The Notifying Party states that in past Commission decisions, and in particular M.9424 – NVIDIA/Mellanox, and M.10097 – AMD/XILINX, the Commission has taken the view that different processor types do not compete with each other. According to the Notifying Party, the above Commission precedents apply *mutatis mutandis* to processor IP, that shall therefore be segmented by processor type, resulting in separate relevant markets for CPU IP, GPU IP, DSP IP, NPU IP and ISP IP.. . In any event, the Notifying Party submits that the exact market definition can be left open as the Transaction does not give rise to competition concerns under any plausible definition.[106]

(100) In respect of interface IP, the Notifying Party claims that all interface IP products meet the same broad customer need. More specifically, the Notifying Party submits that from a demand-side perspective, all interface IP products ensure compatibility with industry standard interface protocols. Furthermore, from a supply-side perspective, most interface IP licensors are active across multiple interface protocols. In any event, the Notifying Party submits that the exact market definition can be left open as the Transaction does not give rise to competition concerns under any plausible definition.[107]

(101) Regarding foundation IP, the Notifying Party states that products can be further split into memory IP and physical library IP. Moreover, the Notifying Party submits that within memory IP a further sub segmentation could be considered between embedded memory IP and non-volatile memory ('NVM') IP. In any event, the Notifying Party considers that the exact scope of the market can be left open as

104 Replies to questionnaire to customers of EDA and design IP, question D.A.A. to D.A.F.
105 Commission decision of 23 November 2015 in Case M.7876 – *Avago/Broadcom*.
106 Form CO, Appendix 1 - Intellectual Property business, paragraph 21-22
107 Form CO, Appendix 1 - Intellectual Property business, paragraphs 24-25

the Transaction does not give rise to competition concerns under any plausible definition.[108]

(102) As regards the other IP category, the Notifying Party notes that this "catch-all" category encompasses a wide range of design IP products beyond those in the categories above that provide many disparate functions and therefore does not consider this category to be a relevant product market. The Notifying Party submits that within the other IP category a potential distinction could be made between security IP and other types of IP. In any event, the Notifying Party considers that the exact scope of the market can be left open as the Transaction does not give rise to competition concerns under any plausible definition.[109]

4.3.1.3. Commission's assessment

(103) The Commission has looked at a plausible further segmentation of each of the categories mentioned at Section 4.3.1.2, based on the function performed by the design IP in question. Concretely, as regards processor IP, the Commission has looked at plausible markets per type of processor IP, which are mentioned in the above Section. As regards foundation IP, the Commission has looked at plausible markets for embedded memories, for NVM memory IP and for physical libraries. As regards interface IP, the Commission has looked at plausible markets for wired interface IP on the one hand, and for wireless interface IP on the other hand. As regards other IP, the Commission has looked at a plausible market for security IP that is separate from other design IP products. This approach largely reflects the views expressed by a market participant.[110] Further, the results of the market investigation did not suggest any alternative product market definitions.

(104) For the purposes of this Decision, the Commission concludes that the precise product market definition for design IP can be left open, as the Transaction does not raise serious doubts as to its compatibility with the internal market under any of the above-mentioned plausible product market definitions.[111]

4.3.2. Geographic market definition

4.3.2.1. Past Commission decisions

(105) In M.7686 – Broadcom/Avago the Commission concluded that the relevant geographic markets for SerDes IP licensing should be considered worldwide in scope.

4.3.2.2. The Notifying Party's views

(106) The Notifying Party submits that competition in design IP takes place at a global level since customers purchase products from suppliers irrespective of their location and providers offer design IP products globally. The Notifying Party

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108 Form CO, Appendix 1 - Intellectual Property business, paragraphs 27-28

109 Form CO, Appendix 1 - Intellectual Property business, paragraphs 29-31.

110 Agreed minutes of the conference call of 27 June 2024 with a market participant, para. 22.

111 Ansys does not offer any design IP products and is therefore not active in any of these plausible markets. Further, regardless of the product market definition, the assessment of the conglomerate concerns raised in this Decision does not change.

therefore submits that the appropriate geographic market for design IP products is global.[112]

4.3.2.3. Commission's assessment

(107) For the purposes of this Decision and in line with the above-mentioned precedent, the Commission concludes that the geographic scope of the relevant markets for design IP, regardless of the exact definition at product level, is worldwide.

5. COMPETITIVE ASSESSMENT

5.1. Introduction and identification of affected markets

(108) Under Article 2(2) and (3) of the Merger Regulation, the Commission must assess whether a proposed concentration would significantly impede effective competition in the internal market or in a substantial part of it, in particular through the creation or strengthening of a dominant position.

(109) In this respect, a merger may entail horizontal and/or non-horizontal (namely, vertical or conglomerate) effects. Horizontal effects are those deriving from a concentration where the undertakings concerned are actual or potential competitors of each other in one or more of the relevant markets concerned. Vertical effects are those deriving from a concentration where the undertakings concerned are active on different or multiple levels of the supply chain. Conglomerate effects are those deriving from a concentration where the undertakings concerned are in a relationship which is neither horizontal nor vertical. A concentration may involve all three types of effects. In such a case, the Commission will appraise horizontal and non-horizontal effects in accordance with the guidance set out in the relevant notices, that is to say the Horizontal Merger Guidelines[113] and the Non-Horizontal Merger Guidelines.[114]

(110) In assessing the competitive effects of a merger, the Commission compares the competitive conditions that would result from the notified merger with the conditions that would have prevailed without the merger. In most cases, the competitive conditions existing at the time of the merger constitute the relevant comparison for evaluating the effects of a merger. However, in some circumstances, the Commission may take into account future changes to the market that can reasonably be predicted.[115]

(111) As explained in Section 4, for the purposes of the present Decision, the Commission will conduct its competitive assessment in the markets, which correspond to the EDA functions listed in Table 8 of Annex A, and which are identified as affected in the present section.

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112 Form CO, Appendix 1 - Intellectual Property business, paragraph 32.

113 Guidelines on the assessment of horizontal mergers under the Council Regulation on the control of concentrations between undertakings ("**Horizontal Merger Guidelines**"), OJ C31, 5.2.2004, p. 5.

114 Guidelines on the assessment of non-horizontal mergers under the Council Regulation on the control of concentrations between undertakings ("**Non-Horizontal Merger Guidelines**"), OJ C 265, 190.2008.

115 Horizontal Merger Guidelines, paragraph 9; Non-Horizontal Merger Guidelines, paragraph 20.

5.1.1. Horizontally affected markets

(112) The Parties' activities horizontally overlap in the markets for optics software, for photonics software as well as in several EDA markets. As a result, the Transaction gives rise to the following **horizontally affected markets**, i.e., markets in which both Parties are active and where the combined market shares of the Parties exceed 20% worldwide by revenue in 2023:

Optics and photonics markets

(a) The global market for the supply of optics software;

(b) The global market for the supply of photonics software;

EDA markets

(c) The global market for the supply of photonic chips simulation software;

(d) The global market for the supply of RTL power consumption analysis tools;

(e) The global market for the supply of transistor-level power integrity analysis tools;

(f) The global market for the supply of ESD analysis tools;

(g) The global market for the supply of power device analysis tools;

(h) The global market for the supply of parasitic analysis tools;

(i) The global market for the supply of functional safety specification and analysis tools;

(113) Regarding the market for the **global supply of gate-level power integrity analysis tools**, the Commission has received a complaint submitting there is an actual horizontal overlap between the Parties' activities in this market.[116] Ansys offers this functionality in its flagship tool RedHawk(-SC), which is the biggest revenue-generating tool of Ansys' semiconductor portfolio. Synopsys does not have its own product, but rather partners with Ansys to offer a lighter, in-design version of this tool (RedHawk Analysis Fusion), which is an add-on to Synopsys' digital IC physical design tools (IC Compiler II and Fusion Compiler).[117] The results of the market investigation have confirmed that the Parties do not compete in this market, as the majority of respondents who expressed a view replied that the RedHawk Analysis Fusion and RedHawk(-SC) serve distinct purposes.[118] Customers have indicated that RedHawk Analysis Fusion is not available as a standalone product but only as part of IC Compiler and Fusion Compiler and that it only delivers "coarse"/in-design analysis and does not offer gate-level power integrity sign-off.[119] Accordingly, the Commission considers this is not a horizontally affected market.

(114) Regarding the design IP markets, the Transaction does not result in any horizontal overlaps in any possible design IP market, as Ansys is not active in the provision of design IP products.

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116 Market participant's written submission received on 14 June 2024.

117 Form CO, para. 409 and 1039. Prior to the partnership with Ansys, Synopsys offered a gate-level power integrity analysis tool (PrimeRail). Synopsys submits that this solution [description of Synopsys assessment of tool capabilities and commercial performance], which led to it being discontinued in 2017, in favour of the partnership.

118 Replies to Questionnaire to customers of EDA and design IP, question D.A.C.4.

119 Replies to Questionnaire to customers of EDA and design IP, question D.A.C.4.1.

5.1.2. Relevant markets for conglomerate effects

(115) The Transaction results in a number of conglomerate relationships between Synopsys' and Ansys' activities in the EDA markets, and between Synopsys' activities in design IP markets on the one hand and Ansys' activities in the EDA markets on the other hand. As a result, the Transaction gives rise to the following **markets relating to conglomerate links between the Parties from which the Merged Entity could potentially leverage its market power ("conglomerate leveraging markets")**, i.e., markets where the individual or combined market shares of the Parties exceed 30% worldwide by revenue in 2023 and in which at least one Party is active whilst the other Party is active on a neighbouring market:[120]

EDA markets

(a) The global market for the supply of gate-level power integrity analysis tools;

(b) The global market for the supply of gate-level security analysis tools;

(c) The global market for the supply of structural and thermal analysis tools;

(d) The global market for the supply of clock jitter analysis tools;

(e) The global market for the supply of electromagnetic simulation tools;

(f) The global market for the supply of signal and power integrity tools;

(g) The global market for the supply of parasitic analysis tools;

(h) The global market for the supply of power device analysis tools;

(i) The global market for the supply of RTL power consumption analysis tools;

(j) The global market for the supply of transistor-level power integrity analysis tools;

(k) The global market for the supply of RTL analysis tools;

(l) The global market for the supply of timing analysis tools;

(m) The global market for the supply of design robustness tools;

(n) The global market for the supply of ECO tools;

(o) The global market for the supply of debug verification tools;

(p) The global market for the supply of gate-level power consumption analysis tools;

(q) The global market for the supply of RTL synthesis tools;

(r) The global market for the supply of parasitic extraction tools;

(s) The global market for the supply of characterisation tools;

(t) The global market for the supply of place and route tools;

(u) The global market for the supply of hardware-assisted verification tools;

(v) The global market for the supply of simulation verification tools;

(w) The global market for the supply of circuit simulation tools;

120 The markets neighbouring or with conglomerate links to these conglomerate leveraging markets are listed in Annex A, which lists all interoperability pairs stemming from these conglomerate leveraging markets.

(x) The global market for the supply of virtual prototyping tools;

(y) The global market for the supply of TCAD;

(z) The global market for the supply of Synthesis tools;

(aa) The global market for the supply of static verification tools;

(bb) The global market for the supply of equivalence checking tools;

(cc) The global market for the supply of FPGA Synthesis tools;

(dd) The global market for the supply of silicon lifecycle management IP tools;

(ee) The global market for the supply of timing constraints tools;

(ff) The global market for the supply of design-for-test/Test IP tools;

(gg) The global market for the supply of HAT tools;

Design IP markets

(hh) The global market for the supply of embedded memories;

(ii) The global market for the supply of physical libraries;

(jj) The global market for the supply of wired interface IP.

(116) Each of these potential effects is discussed in turn in the following sections. After setting out the market shares in the relevant markets (Section 5.2), the Commission will first assess the potential horizontal non-coordinated effects stemming from the Transaction (Section 5.3). Second, the Commission will assess the potential conglomerate non-coordinated effects stemming from the Transaction (Section 5.4).

5.2. Market shares

(117) According to the Horizontal Merger Guidelines and the Non-Horizontal Merger Guidelines,[121] in the assessment of the effects of a merger, market shares constitute a useful first indication of the structure of the markets at stake and of the competitive importance of the relevant market players.

(118) In the following tables, the Commission presents the market shares of the Parties in all of the markets listed in Section 5.1 above.

5.2.1. Global market for the supply of optics software

(119) The following table contains the market shares in the global market for the supply of optics software from 2021 to 2023.

Table 1: Market shares in the global market for the supply of optics software by value (2021-2023)

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[30-40]%	[…]	[30-40]%	[…]	[40-50]%
ANSYS	[…]	[50-60]%	[…]	[60-70]%	[…]	[60-70]%
COMBINED	[…]	[90-100]%	[…]	[90-100]%	[…]	[90-100]%

[121] Horizontal Merger Guidelines, paragraph 14; Non-Horizontal Merger Guidelines, paragraph 24.

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
OTHERS[122]	[…]	[5-10]%	[…]	[0-5]%	[…]	[0-5]%
TOTAL[123]	[…]	100%	[…]	100%	[…]	100%
POST-HHI		[…]		[…]		[…]
POST-HHI**		[…]		[…]		[…]
DELTA-HHI		[…]		[…]		[…]

Source: Form CO, Table 48.
**Others are treated as a single undertaking **Others assumed to be infinitesimally small.*

(120) The table above shows that that the Transaction will essentially create a monopolist on the global market for the supply of optics software. Furthermore, the table above shows that the Parties have consistently strengthened their individual market position since 2021, with the effect of shrinking the share of the market addressed by other providers of optics software.

5.2.2. Global market for the supply of photonics software

(121) The following table contains the market shares in the global market for the supply of photonics software from 2021 to 2023.

Table 2: Market shares in the global market for the supply of photonics software by value (2021-2023)

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[10-20]%	[…]	[10-20]%	[…]	[10-20]%
ANSYS	[…]	[60-70]%	[…]	[50-60]%	[…]	[40-50]%
COMBINED	[…]	[80-90]%	[…]	[70-80]%	[…]	[60-70]%
OTHERS[124]	[…]	[10-20]%	[…]	[20-30]%	[…]	[30-40]%
TOTAL[125]	[…]	100%	[…]	100%	[…]	100%
POST-HHI*		[…]		[…]		[…]
POST-HHI**		[…]		[…]		[…]
DELTA-HHI		[…]		[…]		[…]

Source: Form CO, Table 47.
**Others are treated as a single undertaking **Others assumed to be infinitesimally small.*

(122) The table above shows that that the Transaction will create a clear market leader on the global market for the supply of photonics software. While Synopsys' market share has remained relatively stable, the table above shows that Ansys' market share has declined since 2021. Accordingly, the combined market share of the Parties has been shrinking since 2021 but remains significantly above 50%.

5.2.3. Global markets for EDA

5.2.3.1. Horizontally affected EDA markets where the Parties' combined market share exceeds 25% and HHI Delta is above 150.

(123) This Section presents market shares in the 7 horizontally affected EDA markets, where the Parties have a combined market share above 50% or a combined market share of 25% worldwide by revenue in 2023 or above and a Delta-HHI of 150 or

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122 According to the Notifying Party, this includes: Photon Engineering, COMSOL Multiphysics, Breault Research Organization, Lambda Research Corporation, Autodesk, Quadoa Optical Systems, LightTrans, Silvaco.

123 The total market share may exceed 100 due to rounding.

124 According to the Notifying Party, this includes: VPIphotonics, Photon Design, Optiwave Systems, CrossLight Software, Dassault Systèmes, JCM wave, Flexcompute, LightTrans, COMSOL Multiphysics, Fluxim.

125 The total market share may exceed 100 due to rounding.

above, as well as an additional EDA tool market, ESD Analysis, for which the Commission was informed of specific concerns raised by a market participant:[126,127]

(a) Table 3 – RTL Power Consumption Analysis (Functional ID 3);

(b) Table 4 – Electrostatic discharge (ESD) Analysis (Functional ID 22);[128]

(c) Table 5 – Parasitic Analysis (Functional ID 28);

(d) Table 6 – Transistor-level Power Integrity Analysis (Functional ID 41);

(e) Table 7 – Power Device Analysis (Functional ID 42);

(f) Table 8 – Photonic Chip Simulation (Functional ID 55);

(g) Table 9 – Functional Safety & Specification Analysis (Functional ID 82).

Table 3. RTL Power Consumption Analysis (Functional ID 3).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[20-30]%	[…]	[20-30]%	[…]	[30-40]%
ANSYS	[…]	[30-40]%	[…]	[40-50]%	[…]	[40-50]%
COMBINED	[…]	[60-70]%	[…]	[60-70]%	[…]	[70-80]%
CADENCE	[…]	[10-20]%	[…]	[10-20]%	[…]	[10-20]%
SIEMENS	[…]	[20-30]%	[…]	[10-20]%	[…]	[10-20]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]
DELTA-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 4. ESD Analysis (Functional ID 22).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[10-20]%	[…]	[10-20]%	[…]	[10-20]%
ANSYS	[…]	[10-20]%	[…]	[10-20]%	[…]	[10-20]%
COMBINED	[…]	[20-30]%	[…]	[20-30]%	[…]	[20-30]%
CADENCE	[…]	[5-10]%	[…]	[5-10]%	[…]	[5-10]%
SIEMENS	[…]	[70-80]%	[…]	[60-70]%	[…]	[60-70]%
PRIMARIUS	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
ANGSTROM_DESIGN	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
KEYSIGHT	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]
DELTA-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

126 Commission notice on a simplified treatment for certain concentrations under Council Regulation (EC) No 139/2004 on the control of concentrations between undertakings, para 8(a) and 5(d)i(bb).

127 The market for Parasitic Analysis (Functional ID 28) is not horizontally affected. In 2023, the Parties had a high combined market share of [70-80]% but a Delta-HHI of only […]. In 2021 and 2022 the Delta-HHI was even lower. However, this market is included in the list of non-horizontally affected markets below.

128 This market is not horizontally affected, as the combined market share does not exceed 25%. However, the Commission has assessed the impact of the Transaction in its market investigation, in view of the specific concerns raised by one market participant.

Table 5. Parasitic Analysis (Functional ID 28).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
ANSYS	[…]	[70-80]%	[…]	[60-70]%	[…]	[70-80]%
COMBINED	[…]	[70-80]%	[…]	[60-70]%	[…]	[70-80]%
CADENCE	[…]	[10-20]%	[…]	[10-20]%	[…]	[10-20]%
SIEMENS	[…]	[10-20]%	[…]	[10-20]%	[…]	[10-20]%
SILVACO	[…]	[5-10]%	[…]	[5-10]%	[…]	[0-5]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]
DELTA-HHI		-		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 6. Transistor-level Power Integrity Analysis (Functional ID 41).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
ANSYS	[…]	[30-40]%	[…]	[30-40]%	[…]	[40-50]%
COMBINED	[…]	[40-50]%	[…]	[40-50]%	[…]	[40-50]%
CADENCE	[…]	[40-50]%	[…]	[40-50]%	[…]	[40-50]%
SIEMENS	[…]	[0-5]%	[…]	[0-5]%	[…]	[5-10]%
MATHWORKS	-	[0-5]%	[…]	[0-5]%	[…]	[5-10]%
EMPYREAN	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
SIGASI	[…]	[5-10]%	[…]	[0-5]%	-	[0-5]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]
DELTA-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 7. Power Device Analysis (Functional ID 42).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[40-50]%	[…]	[40-50]%	[…]	[40-50]%
ANSYS	-	[0-5]%	[…]	[5-10]%	[…]	[5-10]%
COMBINED	[…]	[40-50]%	[…]	[40-50]%	[…]	[40-50]%
JEDAT	[…]	[30-40]%	[…]	[20-30]%	[…]	[20-30]%
EMPYREAN	[…]	[0-5]%	[…]	[5-10]%	[…]	[10-20]%
PRIMARIUS	[…]	[10-20]%	[…]	[10-20]%	[…]	[10-20]%
SIGASI	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]
DELTA-HHI		-		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 8. Photonic Chip Simulation (Functional ID 55).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[10-20]%	[…]	[10-20]%	[…]	[10-20]%
ANSYS	[…]	[20-30]%	[…]	[10-20]%	[…]	[10-20]%
COMBINED	[…]	[40-50]%	[…]	[20-30]%	[…]	[20-30]%
VPI PHOTONICS	[…]	[5-10]%	[…]	[10-20]%	[…]	[10-20]%
OPTIWAVE	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
PHOTON DESIGN	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
CADENCE	[…]	[30-40]%	[…]	[30-40]%	[…]	[30-40]%
SIEMENS	[…]	[5-10]%	[…]	[5-10]%	[…]	[5-10]%
KEYSIGHT	[…]	[5-10]%	[…]	[10-20]%	[…]	[10-20]%
EMPYREAN	[…]	[0-5]%	[…]	[5-10]%	[…]	[5-10]%
LATITUDE DESIGN SYSTEMS		[0-5]%		[0-5]%		[0-5]%
TOTAL	[…]	100%	[…]	100%	[…]	100%
POST-HHI		[…]		[…]		[…]
DELTA-HHI		[…]		[…]		[…]

Source: Reply to RFI 25, Table 3, Commission assessment.

Table 9. Functional Safety & Specification Analysis (Functional ID 82).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[10-20]%	[…]	[5-10]%	[…]	[10-20]%
ANSYS	[…]	[10-20]%	[…]	[10-20]%	[…]	[10-20]%
COMBINED	[…]	[20-30]%	[…]	[20-30]%	[…]	[20-30]%
CADENCE	[…]	[50-60]%	[…]	[40-50]%	[…]	[40-50]%
SIEMENS	[…]	[20-30]%	[…]	[20-30]%	[…]	[20-30]%
ENCO SAFETY OFFICE	-	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
PLATO	-	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
ISOGRAPH	-	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
APIS	-	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
VECTOR	-	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
C2A	-	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]
DELTA-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

5.2.3.2. Other EDA markets in which the Transaction may have an impact due to potential competition

(124) This Section lists market shares in the two global EDA markets in which the Transaction may be impacted due to potential competition between the Parties:

(a) Table 10 – Structural and Thermal Analysis (Functional ID 75);

(b) Table 11 – Signal and Power Integrity (Functional ID 76);

Table 10. Structural and Thermal Analysis (Functional ID 75).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
ANSYS	[…]	[50-60]%	[…]	[70-80]%	[…]	[70-80]%
CADENCE	[…]	[30-40]%	[…]	[20-30]%	[…]	[20-30]%
SIEMENS	[…]	[10-20]%	[…]	[10-20]%	[…]	[10-20]%
TOTAL	[…]		[…]		[…]	
POST-HHI	[…]	[…]	[…]	[…]	[…]	[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 11. Signal and Power Integrity (Functional ID 76).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
ANSYS	[…]	[30-40]%	[…]	[30-40]%	[…]	[30-40]%
CADENCE	[…]	[40-50]%	[…]	[40-50]%	[…]	[40-50]%
KEYSIGHT	[…]	[5-10]%	[…]	[5-10]%	[…]	[10-20]%
LORENTZ	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
MATHWORKS	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
EMPYREAN	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
ALTIUM	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
ZUKEN	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

5.2.3.3. Conglomerate leveraging EDA markets where Ansys individually holds more than 30% market share

(125) This Section lists market shares in the 4 global conglomerate leveraging EDA markets where Ansys individually holds a market share of more than 30%

worldwide by revenue in 2023, and because the Parties are active in neighbouring markets:[129]

(a) Table 12 – Clock Jitter Analysis (Functional ID 25);

(b) Table 13 – Gate-level Power Integrity Analysis (Functional ID 30);

(c) Table 14 – Gate-level Security Analysis (Functional ID 31);

(d) Table 15 – Electromagnetic Simulation (Functional ID 49);

Table 12. Clock Jitter Analysis (Functional ID 25).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
ANSYS	[…]	[30-40]%	[…]	[40-50]%	[…]	[30-40]%
CADENCE	[…]	[30-40]%	[…]	[20-30]%	[…]	[30-40]%
SIEMENS	[…]	[30-40]%	[…]	[20-30]%	[…]	[30-40]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 13. Gate-level Power Integrity Analysis (Functional ID 30).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
ANSYS	[…]	[60-70]%	[…]	[60-70]%	[…]	[50-60]%
CADENCE	[…]	[30-40]%	[…]	[30-40]%	[…]	[30-40]%
SIEMENS	[…]	[5-10]%	[…]	[5-10]%	[…]	[5-10]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 14. Gate-level Security Analysis (Functional ID 31).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
ANSYS	[…]	[90-100]%	[…]	[90-100]%	[…]	[90-100]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 15. Electromagnetic Simulation (Functional ID 49).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
ANSYS	[…]	[50-60]%	[…]	[50-60]%	[…]	[50-60]%
CADENCE	[…]	[20-30]%	[…]	[20-30]%	[…]	[30-40]%
KEYSIGHT	[…]	[10-20]%	[…]	[10-20]%	[…]	[10-20]%
DASSAULT	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

[129] Note that in addition, Ansys holds a market share of 30% or above in the horizontally affected markets RTL Power Consumption Analysis (Functional ID 3), Parasitic Analysis (Functional ID 28) and Transistor-level Power Integrity Analysis (Functional ID 41) and in the markets affected due to potential competition, Structural and Thermal Analysis (Functional ID 75) and Signal and Power Integrity (Functional ID 76). For the avoidance of doubt, there are no markets where the Parties' combined market share exceeds 30% and Synopsys'/Ansys' individual market share does not exceed 30%.

5.2.3.4. Conglomerate leveraging EDA markets where Synopsys individually holds more than 30% market share

(126) This Section lists market shares in the 23 global conglomerate leveraging EDA markets where Synopsys individually holds a market share of more than 30% worldwide by revenue in 2023, and because the Parties are active in neighbouring markets:[130]

(a) Table 16 – RTL Analysis (Functional ID 2);

(b) Table 17 – RTL Synthesis (Functional ID 5);

(c) Table 18 – FPGA Synthesis (Functional ID 6);

(d) Table 19 – Static Verification (Functional ID 7);

(e) Table 20 – Gate-level Power Consumption Analysis (Functional ID 8);

(f) Table 21 –Timing Constraints (Functional ID 9);

(g) Table 22 – Silicon Lifecycle Management IP (Functional ID 10);

(h) Table 23 –Design-for-Test / Test IP (Functional ID 11);

(i) Table 24 – Simulation Verification (Functional ID 12);

(j) Table 25 – Debug Verification (Functional ID 13);

(k) Table 26 – Hardware-Assisted Verification (Functional ID 17);

(l) Table 27 – Place & Route (Functional ID 18);

(m) Table 28 – Equivalence Checking (Functional ID 20);

(n) Table 29 – Timing Analysis (Functional ID 23);

(o) Table 30 – ECO (Functional ID 24);

(p) Table 31 – Parasitic Extraction (Functional ID 27);

(q) Table 32 – Design Robustness (Functional ID 29);

(r) Table 33 – Circuit Simulation (Functional ID 33);

(s) Table 34 – Characterisation (Functional ID 81);

(t) Table 35 – HAT (Functional ID 83);

(u) Table 36 – Synthesis (Functional ID 85);

(v) Table 37 – TCAD (Functional ID 86);

(w) Table 38 – Virtual Prototyping (Functional ID 87);

Table 16. RTL Analysis (Functional ID 2).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[90-100]%	[…]	[90-100]%	[…]	[90-100]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

130 Note that in addition, Synopsys holds a market share of 30% or above in the horizontally affected market Power Device Analysis (Functional ID 42). For the avoidance of doubt, there are no markets where the Parties' combined market share exceeds 30% and Synopsys'/Ansys' individual market share does not exceed 30%.

Table 17. RTL Synthesis (Functional ID 5).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[70-80]%	[…]	[60-70]%	[…]	[60-70]%
CADENCE	[…]	[20-30]%	[…]	[30-40]%	[…]	[30-40]%
SIEMENS	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 18. FPGA Synthesis (Functional ID 6).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[80-90]%	[…]	[50-60]%	[…]	[50-60]%
SIEMENS	[…]	[5-10]%	[…]	[10-20]%	[…]	[10-20]%
ALTERA	[…]	[5-10]%	[…]	[10-20]%	[…]	[10-20]%
AMD	[…]	[0-5]%	[…]	[5-10]%	[…]	[5-10]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 19. Static Verification (Functional ID 7).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[50-60]%	[…]	[60-70]%	[…]	[60-70]%
CADENCE	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
SIEMENS	[…]	[20-30]%	[…]	[10-20]%	[…]	[5-10]%
REAL_INTENT	[…]	[10-20]%	[…]	[20-30]%	[…]	[10-20]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 20. Gate-level Power Consumption Analysis (Functional ID 8).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[80-90]%	[…]	[70-80]%	[…]	[70-80]%
CADENCE	[…]	[10-20]%	[…]	[20-30]%	[…]	[20-30]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 21. Timing Constraints (Functional ID 9).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[60-70]%	[…]	[50-60]%	[…]	[40-50]%
CADENCE	[…]	[20-30]%	[…]	[20-30]%	[…]	[20-30]%
AUSDIA	[…]	[0-5]%	[…]	[10-20]%	[…]	[10-20]%
EXCELLION	[…]	[0-5]%	[…]	[10-20]%	[…]	[10-20]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 22. Silicon Lifecycle Management IP (Functional ID 10).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[40-50]%	[…]	[40-50]%	[…]	[50-60]%
SIEMENS	[…]	[20-30]%	[…]	[20-30]%	[…]	[10-20]%
PROTEANTECS	[…]	[30-40]%	[…]	[30-40]%	[…]	[30-40]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 23. Design-for-Test/Test IP (Functional ID 11).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[30-40]%	[…]	[30-40]%	[…]	[30-40]%
CADENCE	[…]	[10-20]%	[…]	[10-20]%	[…]	[10-20]%
SIEMENS	[…]	[40-50]%	[…]	[40-50]%	[…]	[40-50]%
SYNTEST	[…]	[0-5]%	[…]	[5-10]%	[…]	[5-10]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 24. Simulation Verification (Functional ID 12).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[30-40]%	[…]	[30-40]%	[…]	[30-40]%
CADENCE	[…]	[30-40]%	[…]	[30-40]%	[…]	[30-40]%
SIEMENS	[…]	[20-30]%	[…]	[20-30]%	[…]	[20-30]%
CAST	[…]	[5-10]%	[…]	[0-5]%	[…]	[5-10]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 25. Debug Verification (Functional ID 13).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[80-90]%	[…]	[70-80]%	[…]	[70-80]%
CADENCE	[…]	[5-10]%	[…]	[10-20]%	[…]	[10-20]%
SIEMENS	[…]	[0-5]%	[…]	[10-20]%	[…]	[10-20]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 26. Hardware-Assisted Verification (Functional ID 17).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[40-50]%	[…]	[40-50]%	[…]	[40-50]%
CADENCE	[…]	[30-40]%	[…]	[40-50]%	[…]	[40-50]%
SIEMENS	[…]	[10-20]%	[…]	[10-20]%	[…]	[10-20]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 27. Place & Route (Functional ID 18).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[50-60]%	[…]	[40-50]%	[…]	[40-50]%
CADENCE	[…]	[40-50]%	[…]	[50-60]%	[…]	[50-60]%
SIEMENS	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
EMPYREAN	[…]	[0-5]%	[…]	[0-5]%	-	[0-5]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 28. Equivalence Checking (Functional ID 20).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[40-50]%	[…]	[30-40]%	[…]	[30-40]%
CADENCE	[…]	[50-60]%	[…]	[60-70]%	[…]	[50-60]%
SIEMENS	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 29. Timing Analysis (Functional ID 23).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[80-90]%	[…]	[80-90]%	[…]	[80-90]%
CADENCE	[…]	[10-20]%	[…]	[5-10]%	[…]	[5-10]%
SIEMENS	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
EMPYREAN	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 30. ECO (Functional ID 24).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[80-90]%	[…]	[80-90]%	[…]	[80-90]%
CADENCE	[…]	[10-20]%	[…]	[10-20]%	[…]	[10-20]%
SIEMENS	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
EMPYREAN	[…]	[5-10]%	[…]	[5-10]%	[…]	[5-10]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 31. Parasitic Extraction (Functional ID 27).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[40-50]%	[…]	[40-50]%	[…]	[40-50]%
CADENCE	[…]	[40-50]%	[…]	[40-50]%	[…]	[40-50]%
SIEMENS	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
EMPYREAN	[…]	[0-5]%	[…]	[5-10]%	[…]	[0-5]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 32. Design Robustness (Functional ID 29).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[70-80]%	[…]	[70-80]%	[…]	[70-80]%
CADENCE	[…]	[10-20]%	[…]	[10-20]%	[…]	[10-20]%
SIEMENS	[…]	[10-20]%	[…]	[10-20]%	[…]	[5-10]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 33. Circuit Simulation (Functional ID 33).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[40-50]%	[…]	[30-40]%	[…]	[30-40]%
CADENCE	[…]	[40-50]%	[…]	[40-50]%	[…]	[30-40]%
SIEMENS	[…]	[5-10]%	[…]	[5-10]%	[…]	[5-10]%
MATHWORKS	-	[0-5]%	[…]	[10-20]%	[…]	[10-20]%
EMPYREAN	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 34. Characterisation (Functional ID 81).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[40-50]%	[…]	[40-50]%	[…]	[40-50]%
CADENCE	[…]	[30-40]%	[…]	[40-50]%	[…]	[40-50]%
SIEMENS	[…]	[10-20]%	[…]	[10-20]%	[…]	[10-20]%
EMPYREAN	[…]	[0-5]%	[…]	[0-5]%	-	[0-5]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 35. HAT (Functional ID 83).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[80-90]%	[…]	[90-100]%	[…]	[90-100]%
SIEMENS	[…]	[10-20]%	[…]	[0-5]%	[…]	[10-20]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 36. Synthesis (Functional ID 85).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[30-40]%	[…]	[30-40]%	[…]	[30-40]%
CADENCE	[…]	[60-70]%	[…]	[60-70]%	[…]	[60-70]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 37. TCAD (Functional ID 86).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[70-80]%	[…]	[70-80]%	[…]	[80-90]%
LAM	[…]	[10-20]%	[…]	[10-20]%	[…]	[10-20]%
SILVACO	[…]	[10-20]%	[…]	[5-10]%	[…]	[5-10]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 38. Virtual Prototyping (Functional ID 87).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[60-70]%	[…]	[70-80]%	[…]	[80-90]%
CADENCE	[…]	[10-20]%	[…]	[10-20]%	[…]	[5-10]%
SIEMENS	[…]	[5-10]%	[…]	[5-10]%	[…]	[0-5]%
MATHWORKS	[…]	[10-20]%	[…]	[5-10]%	[…]	[0-5]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

5.2.4. Global markets for Design IP

(127) This Section lists market shares in the three global design IP conglomerate leveraging markets where Synopsys individually holds a market share of more than 30% worldwide by revenue in 2023, and because the Parties are active in neighbouring markets:

(a) Table 39 – Embedded Memories (Functional ID 89);

(b) Table 40 – Physical Libraries (Functional ID 91);

(c) Table 41 – Wired interface IP (Functional ID 92);

Table 39. Embedded Memories (Functional ID 89).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[50-60]%	[…]	[50-60]%	[…]	[50-60]%
ARM	[…]	[20-30]%	[…]	[20-30]%	[…]	[20-30]%
M31	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
OTHERS	[…]	[20-30]%	[…]	[20-30]%	[…]	[20-30]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 40. Physical Libraries (Functional ID 91).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[30-40]%	[…]	[30-40]%	[…]	[30-40]%
ARM	[…]	[30-40]%	[…]	[30-40]%	[…]	[30-40]%
VERISILICON	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
ARAGIO	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
OTHERS	[…]	[20-30]%	[…]	[20-30]%	[…]	[20-30]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

Table 41. Wired Interface IP (Functional ID 92).

Firm	Revenue 2021 (USD […])	Share 2021 (%)	Revenue 2022 (USD […])	Share 2022 (%)	Revenue 2023 (USD […])	Share 2023 (%)
SYNOPSYS	[…]	[50-60]%	[…]	[50-60]%	[…]	[60-70]%
CADENCE	[…]	[10-20]%	[…]	[10-20]%	[…]	[10-20]%
ALPHAWAVE	[…]	[5-10]%	[…]	[5-10]%	[…]	[5-10]%
RAMBUS	[…]	[0-5]%	[…]	[0-5]%	[…]	[0-5]%
OTHERS	[…]	[20-30]%	[…]	[20-30]%	[…]	[10-20]%
TOTAL	[…]		[…]		[…]	
POST-HHI		[…]		[…]		[…]

Source: Annex RFI 18 Q.4.1, Commission assessment.

5.3. Horizontal non-coordinated effects[131]

5.3.1. Legal framework

(128) The Horizontal Merger Guidelines describe horizontal non-coordinated effects as follows: "*A merger may significantly impede effective competition in a market by removing important competitive constraints on one or more sellers who consequently have increased market power. The most direct effect of the merger will be the loss of competition between the merging firms. For example, if prior to the merger one of the merging firms had raised its price, it would have lost some sales to the other merging firm. The merger removes this particular constraint. Non-merging firms in the same market can also benefit from the reduction of competitive pressure that results from the merger, since the merging firms' price increase may switch some demand to the rival firms, which, in turn, may find it profitable to increase their prices. The reduction in these competitive constraints could lead to significant price increases in the relevant market*".[132]

(129) Generally, a merger giving rise to such non-coordinated effects would significantly impede effective competition by creating or strengthening of the dominant position of a single firm, one which, typically, would have an appreciably larger market share than the next competitor post-merger.

(130) However, under the substantive test set out in Article 2(2) and (3) of the Merger Regulation, mergers that do not lead to the creation or the strengthening the dominant position of a single firm may create competition concerns in oligopolistic markets. Indeed, the Merger Regulation recognises that in oligopolistic markets, it is all the more necessary to maintain effective competition.[133] This is in view of the more significant consequences that mergers may have on such markets. For this reason, the Merger Regulation provides that: "*under certain circumstances, concentrations involving the elimination of important competitive constraints that the merging parties had exerted upon each other, as well as a reduction of competitive pressure on the remaining competitors, may, even in the absence of a likelihood of coordination between the members of the oligopoly, result in a significant impediment to effective competition*."[134]

(131) Paragraph 24 of the Horizontal Merger Guidelines, which sets out the economic rationale underlying non-coordinated anti-competitive effects in horizontal mergers, states that a merger may significantly impede effective competition in a

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131 The Commission has also assessed whether the Transaction is likely to give rise to horizontal coordinated effects on all the markets horizontally affected by the Transaction. However, the Commission has come to the conclusion that the Transaction is unlikely to give rise to serious doubts as to its compatibility with the internal market as a result of horizontal coordinated effects on all horizontally affected markets for the following reasons. First, all horizontally affected markets are growing markets with unstable demand, which are generally less susceptible to competitors coordinating. Second, the Commission's market investigation has not yielded any evidence suggesting that any of the horizontally affected markets are transparent. Third, some of the horizontally affected markets, for instance, the global market for transistor-level power integrity analysis software, are characterised by recent and disruptive entry. As such, the Commission concludes that the Transaction is unlikely to give rise to serious doubts as to its compatibility with the internal market as a result of horizontal coordinated effects on any horizontally affected market.

132 Horizontal Merger Guidelines, para. 24.

133 Merger Regulation, recital 25.

134 Merger Regulation, recital 25. Similar wording is also found in para. 25 of the Horizontal Merger Guidelines.

market by removing important competitive constraints on one or more firms. This paragraph furthermore clarifies that the most direct effect of the merger will be the loss of competition between the merging firms. In order to assess whether a notified merger will result in a significant impediment of effective competition on the basis of non-coordinated effects, the Commission therefore needs to analyse primarily the extent of the competitive constraint imposed pre-merger by each of the merging parties on each other. The following sentence of paragraph 24 of the Horizontal Merger Guidelines clarifies that the removal of the rivalry between the parties may have consequences also on the other players, who may find it profitable to increase their prices. The ultimate effect would thus typically be price increases by the merging parties but also by competitors in the relevant market.

(132) The Commission carries out an overall assessment of the likely effects of the Transaction arising from the elimination of important competitive constraints, taking into consideration the overall body of evidence in its file. The conclusion that a transaction leads to a significant impediment of effective competition is reached taking into account the degree to which all the relevant factors, including the ones listed in paragraphs 27 to 38 of the Horizontal Merger Guidelines, are present in the case under consideration.

(133) The Horizontal Merger Guidelines list a number of factors which may influence whether or not significant horizontal non-coordinated effects are likely to result from a merger. However, not all of these factors need to be present to make significant non-coordinated effects likely and it is not an exhaustive list.[135]

(134) The factors listed in the Horizontal Merger Guidelines include: the large market shares of the merging firms; the fact that the merging firms are close competitors; the limited possibilities for customers to switch suppliers; the fact that the merged entity would be able to hinder expansion by competitors; and the fact that the merger would eliminate an important competitive force.[136]

(135) As regards the elimination of an important competitive force, according to the Horizontal Merger Guidelines, some firms have more of an influence on the competitive process than their market share would suggest. A merger involving such a firm may change the competitive dynamics in a significant anticompetitive way, in particular in a market that is already concentrated.[137] In this respect, paragraph 37 of the Horizontal Merger Guidelines refers to the example of a firm that is a recent entrant on the market and is expected to exert significant competitive pressure in the future. There may, however, also be other situations where a merger may lead to significant non-coordinated effects by removing an important competitive force.

(136) Moreover, concentrations where an undertaking already active in a relevant market merges with or acquires a potential competitor in this market can have similar anti-competitive effects to mergers between two undertakings already active in the same relevant market and, thus, significantly impede effective competition, in particular through the creation or the strengthening of a dominant position.[138] Such merger with a potential competitor can generate horizontal anti-competitive effects,

135 Horizontal Merger Guidelines, para. 26.
136 Horizontal Merger Guidelines, paras. 27 et seq.
137 Horizontal Merger Guidelines, para. 37.
138 Horizontal Merger Guidelines, para. 58.

whether non-coordinated or coordinated, if the potential competitor significantly constrains the behaviour of the firms active in the market. This is the case if the potential competitor possesses assets that could easily be used to enter the market without incurring significant sunk costs. Anti-competitive effects may also occur where the merging partner is very likely to incur the necessary sunk costs to enter the market in a relatively short period of time after which this company would constrain the behaviour of the firms currently active in the market .[139]

(137) For a merger with a potential competitor to have significant anti-competitive effects, two basic conditions must be fulfilled. Firstly, the potential competitor must already exert a significant constraining influence or there must be a significant likelihood that it would grow into an effective competitive force. Secondly, there must not be a sufficient number of other potential competitors, which could maintain sufficient competitive pressure after the merger.[140]

(138) In situations where a merger may result in harmful non-coordinated effects on competition, the Horizontal Merger Guidelines describe a number of factors, which could counteract such harmful effects, that is, the likelihood of buyer power, of entry, as well as efficiencies brought about by the merger.

(139) As regards entry, paragraph 68 of the Horizontal Merger Guidelines provides that when entering a market is sufficiently easy, a merger is unlikely to pose any significant anti-competitive risk. However, for entry to be considered a sufficient competitive constraint on the merging parties, it must be shown to be likely, timely and sufficient to deter or defeat any potential anti-competitive effects of the merger.

5.3.2. Actual horizontal overlaps

5.3.2.1. Global market for the supply of optics software

(140) Optics software are used to simulate the ways in which light behaves in large macro-scale systems involving lenses, mirrors, and prisms in which the system is large enough to allow for light to be modelled as a simple linear ray (also known as ray-tracing).[141]

(141) Both the Notifying Party and Ansys offer optics software. The Notifying Party offers three tools, namely Code V, LightTools and LucidShape. Ansys offers two tools, namely Zemax and Speos.

5.3.2.1.1. The Notifying Party's view

(142) The Notifying Party submits that, although the parties have significant combined market share, the global market for the supply of optics software will continue to be sufficiently competitive post-transaction for the following reasons.

(143) First, although the Parties' solutions overlap, they have different focus areas.[142]

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139 Horizontal Merger Guidelines, para. 59.
140 Horizontal Merger Guidelines, para. 60.
141 Form CO, para. 859.
142 Form CO, para. 962.

(144) Second, the Parties face numerous competitors, including Breault Research Organisation, COMSOL Multiphysics, Lambda Research Corporation, LightTrans and Silvaco, and face competition from in-house solutions.[143]

(145) Third, the Parties face disruptive entrants, including Quadoa Optical Systems and Photon Engineering.[144]

(146) Regardless, the Notifying Party has proposed to divest its optics business in order to remove the overlap between the Parties activities and resolve any potential competition concerns that might be raised by the Transaction.

5.3.2.1.2. The Commission's assessment

(147) The Commission considers that the Transaction raises serious doubts as to its compatibility with the internal market in the global market for the supply of optics software due to horizontal non-coordinated effects for the following reasons.

(148) **First,** the Transaction is likely to lead to the creation or strengthening of a dominant position for the following reasons. The Transaction leads to the creation of a monopolist in the global market for the supply of optics software with a combined market share of 100%. As shown in Table 1 above, in 2023, Synopsys has a market share of [40-50]% and Ansys has a market share of [60-70]% As explained in paragraph 17 of the Horizontal Merger Guidelines, "*According to well-established case law, very large market shares — 50 % or more — may in themselves be evidence of the existence of a dominant market position.*"[145] As explained by one market participant in response to the Commission's market investigation, "*These two actors* [the Parties] *dominate the market for optics/photonics simulation software. Although other providers exist, their products are significantly less well developed. Moving away from Ansys/Synopsys, in the case that they abused their strongly dominant market position as a single entity, would be problematic and costly, although not impossible*."[146]

(149) **Second,** the Transaction is likely to lead to the combination of two close competitors. In particular, a majority of customers of optics software who expressed a view during the Commission's market investigation consider that when deciding which software to use, customers mostly weigh Synopsys' tools with Ansys' tools (and vice-versa).[147]

(150) **Third,** switching is complex and expensive.[148] A majority of customers of optics software who expressed a view during the Commission's market investigation consider that switching provider quickly, easily and without incurring significant costs would not be possible after the Transaction.[149] For instance, one respondent to the Commission's market investigation explains that: "*For optics software, it would not be possible to change (at least in the short to medium term) because we don't know any alternatives*."[150]

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143 Form CO, paras. 963-964.
144 Form CO, para. 965.
145 Horizontal Merger Guidelines, para. 17.
146 Replies to Questionnaire to users and providers of optics and photonics software, question G.1.
147 Replies to Questionnaire to users and providers of optics and photonics software, question E.3.
148 This assessment is made assuming switching to small alternatives or potential new entrants.
149 Replies to Questionnaire to users and providers of optics and photonics software, question E.5.
150 Replies to Questionnaire to users and providers of optics and photonics software, question E.6.

(151) **Fourth,** the Transaction is likely to lead to the elimination of an important innovative competitive force in the global market for the supply of optics software for the following reasons.

(152) In the first place, a majority of customers of optics software who expressed a view in the Commission's market investigation consider that over the past 5 years, Synopsys has innovated in a way that caused changes on the market.[151] For instance, one market participant to the Commission's market investigation explains that: "*Concerning optics software, Code V from Synopsis seems to be updated more frequently than Zemax from Ansys. In addition, Code V unique feature is to take in charge freeforms optics.*"[152]

(153) In the second place, some respondents to the Commission's market investigation expressed concerns that the degree of innovation on the market for the supply of optics software would be reduced after the Transaction. For instance, one market participant explains that: "*We have concerns about the possibility of a price rise, and a lessening of the incentive to provide functional improvements due to the market power of the merged entity. This applies for both Optical Software and Photonics Software (for the use cases relevant to us). Ansys and Synopsys are the sole suppliers of the only viable tools for designing and simulating optical components.*"[153] Another market participant explains that: "*The risk is a lack of involvement and investment in the optical and photonics field and that the lighting part is also neglected.*"[154]

(154) **Fifth,** all potential competitors of the Notifying Party in the global market for the supply of optics software who expressed a view in the Commission's market investigation consider that they would not be able quickly, easily and without incurring significant costs, to start providing optics software to a user who would not wish to source optics software from existing suppliers.[155] This was also confirmed by customers of optics software, a majority of which considers that market entry with a competitive period within two years is unlikely.[156] For instance, one market participant to the Commission's market investigation explains that: "*Optics software : Developing a software as credible as the one of the parties would require significant time and investment.*"[157]

(155) **Sixth,** the results of the market investigation have shown that a majority of customers of optics software would not be able to engage in any counterstrategy to oppose any significant price increase and/or quality degradation by the Merged Entity after the Transaction.[158]

5.3.2.1.3. Conclusion

(156) In view of the above considerations and in light of the results of the market investigation and the evidence and information available to it, the Commission concludes that the Transaction gives rise to serious doubts as to its compatibility

151 Replies to Questionnaire to users and providers of optics and photonics software, question E.7.
152 Replies to Questionnaire to users and providers of optics and photonics software, question E.8.
153 Replies to Questionnaire to users and providers of optics and photonics software, question F.4.
154 Replies to Questionnaire to users and providers of optics and photonics software, question F.4.
155 Replies to Questionnaire to users and providers of optics and photonics software, question D.3.
156 Replies to Questionnaire to users and providers of optics and photonics software, question E.11.
157 Replies to Questionnaire to users and providers of optics and photonics software, question E.12.
158 Replies to Questionnaire to users and providers of optics and photonics software, question E.9.

with the internal market as a result of horizontal non-coordinated effects in the global market for the supply of optics software.

5.3.2.2. Global market for the supply of photonics software

(157) Photonics software is used to simulate the ways in which light behaves in smaller nano-scale optical systems and devices which are smaller than the wavelength of light.

(158) Both the Notifying Party and Ansys offer photonics software. The Notifying Party's product is branded RSoft and Ansys' product is branded Lumerical.

5.3.2.2.1. The Notifying Party's view

(159) The Notifying Party submits that, although the parties have significant combined market share, the global market for the supply of photonics software will continue to be sufficiently competitive post-transaction for the following reasons.

(160) The Notifying Party submits that the Parties face numerous competitors, including VPIphotonics, Photon Design, FlexCompute, COMSOL Multiphysics, CrossLight Software, Fluxim, JCM wave, Optiwave Systems, and face competition from in-house solutions.[159]

(161) Regardless, the Notifying Party has proposed to divest its photonics business in order to remove the overlap between the Parties activities and resolve any potential competition concerns that might be raised by the Transaction.

5.3.2.2.2. The Commission's assessment

(162) The Commission considers that the Transaction raises serious doubts as to its compatibility with the internal market in the global market for the supply of photonics software due to horizontal non-coordinated effects for the following reasons.

(163) **First,** the Transaction is likely to lead to the creation or strengthening of a dominant position for the following reasons. The Transaction leads to a very high combined market share with a sizeable increment in the global market for the supply of photonics software. As shown in Table 2 above, in 2023, the combined market share of the Parties was [60-70]% with an increase of [10-20]% from Synopsy. As explained in paragraph 17 of the Horizontal Merger Guidelines, "*According to well-established case law, very large market shares — 50 % or more — may in themselves be evidence of the existence of a dominant market position.*"[160] As explained by another market participant in response to the Commission's market investigation: "*These two actors* [the Parties] *dominate the market for optics/photonics simulation software. Although other providers exist, their products are significantly less well developed. Moving away from Ansys/Synopsys, in the case that they abused their strongly dominant market position as a single entity, would be problematic and costly, although not impossible*."[161]

159 Form CO, paras. 967-968.
160 Horizontal Merger Guidelines, paragraph 17.
161 Replies to Questionnaire to users and providers of optics and photonics software, question G.1.

(164) **Second,** the Transaction is likely to lead to the combination of two close competitors. In particular, half of the customers of photonics software who expressed a view in the Commission's market investigation consider that when deciding which software to use, customers mostly weigh Synopsys' tools with Ansys' tools (and vice-versa).[162]

(165) **Third,** switching is complex and expensive. A majority of customers of photonics software who expressed a view during the Commission's market investigation consider that switching provider quickly, easily and without incurring significant costs would not be possible after the Transaction.[163] For instance, one respondent to the Commission's market investigation explains that: "*If we had to move from RSoft to another simulation tool (for whatever reason), it would require extra effort and additional training time for the members of the team*."[164] Another customer explained that: "*For photonic software, it will imply* ***high costs and time*** *to transfer all the internal libraries to another tool*."[165] That same market participant explains that: "*For photonics software, the risk on the price is the same than for optics. And, even if alternatives exit, it will be costly and time consuming to switch to another product.*"[166]

(166) **Fourth,** the Transaction is likely to lead to the elimination of an important innovative competitive force on the global market for the supply of photonics software for the following reasons.

(167) In the first place, a majority of customers of photonics software who expressed a view in the Commission's market investigation consider that over the past 5 years, both Synopsys and Ansys have innovated in a way that caused changes on the market.[167] For instance, one market participant to the Commission's market investigation explains that: "*We see both companies as innovative ones, and in the forefront of the field.*"[168]

(168) In the second place, some respondents to the Commission's market investigation expressed concerns that the degree of innovation on the market for the supply of photonics software would be reduced after the Transaction. For instance, one market participant explains that: "*We have concerns about the possibility of a price rise, and a lessening of the incentive to provide functional improvements due to the market power of the merged entity. This applies for both Optical Software and Photonics Software (for the use cases relevant to us). Ansys and Synopsys are the sole suppliers of the only viable tools for designing and simulating optical components.*"[169] Another market participant explains that: "*The risk is a lack of involvement and investment in the optical and photonics field and that the lighting part is also neglected.*"[170]

(169) **Fifth,** all the competitors of the Notifying Party in the global market for the supply of photonics software who expressed a view during the Commission's market

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162 Replies to Questionnaire to users and providers of optics and photonics software, question E.3.
163 Replies to Questionnaire to users and providers of optics and photonics software, question E.5.
164 Replies to Questionnaire to users and providers of optics and photonics software, question E.6.
165 Replies to Questionnaire to users and providers of optics and photonics software, question E.6.
166 Replies to Questionnaire to users and providers of optics and photonics software, question F.4.
167 Replies to Questionnaire to users and providers of optics and photonics software, question E.7.
168 Replies to Questionnaire to users and providers of optics and photonics software, question E.8.
169 Replies to Questionnaire to users and providers of optics and photonics software, question F.4.
170 Replies to Questionnaire to users and providers of optics and photonics software, question F.4.

investigation consider that they would not be able quickly, easily and without incurring significant costs, to start providing a photonics software to a user who would not wish to source a photonics software from existing suppliers.[171]

(170) **Sixth,** the results of the market investigation have shown that a majority of customers of photonics software would not be able to engage in any counterstrategy to oppose any significant price increase and/or quality degradation by the Merged Entity after the Transaction.[172]

5.3.2.2.3. Conclusion

(171) In view of the above considerations and in light of the results of the market investigation and the evidence and information available to it, the Commission concludes that the Transaction gives rise to serious doubts as to its compatibility with the internal market as a result of horizontal non-coordinated effects in the global market for the supply of photonics software.

5.3.2.3. Global market for the supply of photonic chip simulation software

(172) Photonic chips uses photons (particles of light) instead of electrons to transport information. The market for the supply of photonic chip simulation software is still relatively nascent and represents a small fraction of chips, many photonic chip customers are universities or research institutes that use photonic chip design software for research projects.

(173) Photonic chips are designed according to an EDA design flow similar to that of electronic chips. In that respect, some software used in the photonic chip design flow are identical to those used in the electronic analog design flow.

(174) Photonic chip simulation tools allow designers to simulate and analyse the behaviour of a photonic chip to predict and verify the chip's performance. With respect to simulating photonic chips, customers have two options. The first option is the traditional method, which uses a purpose-built photonic chip simulation tool. The second option is to use an electrical circuit simulator, in combination with pre-developed models for the photonic devices in industry-standard Verilog-A language to simulate a photonic chip.

(175) Both the Notifying Party and Ansys offer purpose-built photonic chip simulation tool (Synopsys offers OptSim, and Ansys offers Lumerical INTERCONNECT).[173] In addition, Synopsys' PrimeSim electrical circuit simulator can be used for photonic chip simulation. Ansys does not offer a similar tool.

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171 Replies to Questionnaire to users and providers of optics and photonics software, question D.3.

172 Replies to Questionnaire to users and providers of optics and photonics software, question E.9.

173 Photonic layout design implementation tools, which allow designers to create the layout of a photonic chip, are also purpose-built tools for photonic chips. Synopsys offers OptoCompiler. As Ansys does not have a photonic layout design implementation tool, there is no overlapping activities in this market.

5.3.2.3.1. The Notifying Party's view

(176) The Notifying Party submits that the Transaction will not raise competition concerns in the global market for the supply of photonic chip simulation software for the following reasons.[174]

(177) **First**, the Notifying Party submits that the Parties' combined share in the global market for the supply of photonic chip simulation software will remain modest [20-30]% and the Transaction will result in only a small increment of [10-20]%.

(178) **Second**, the Notifying Party considers that the Parties do not compete closely, as their tools have distinct focuses. Synopsys focuses its competitive efforts on [Synopsys' product-level sale strategies] in the photonic chip design space. Similarly, Ansys focuses its proactive sales of Lumerical INTERCONNECT to [Ansys' product-level sale strategies].

(179) **Third**, the Notifying Party submits that the Merged Entity will continue to face significant competition from at least eight competitors (including three competitors that supply dedicated photonic chip simulation tools and five competitors that supply electrical circuit simulators), including the recent entrant Latitude Design Systems, which introduced PIC Studio, including pSim, in February 2023.

(180) In addition, in the Notifying Party' view, there has been a significant industry trend towards using electrical simulators with Verilog-A models to simulate photonic chips. This transition has been driven by major foundries, which increasingly consider that the best way of achieving photonic chip simulation is simply by extending existing analog workflows to photonic chips. In that respect, the Notifying Party explained that [Synopsys' product plans].

5.3.2.3.2. The Commission's assessment

(181) The Commission considers that the Transaction does not raise serious doubts as to its compatibility with the internal market in the global market for the supply of photonic chip simulation software, for the following reasons.

(182) **First**, the Transaction leads to a moderate combined market share with a limited increment in the global market for the supply of photonic chip simulation software. As shown in table 8 above, in 2023, the Merged Entity's market share was [20-30]%, with an increment of [10-20]%, brought by Synopsys.

(183) In addition, the Commission notes that both Parties' shares have steadily been decreasing over the last three years. Synopsys has lost [5-10], percentage points between 2021 and 2023, while Ansys has lost [5-10] percentage points during the same period.

(184) **Second**, even if the results of the market investigation confirm that the Parties' tools compete, the Commission considers that enough credible alternatives remain in the market for the supply of photonic chip simulation software.

[174] Form CO, paragraphs 526, and seq. Parties' response to the European Commission's RFI 25.

(185) In the first place, while the Notified Party submits that Synopsys and Ansys' tools do not compete, the market investigation shows that the Parties are competitors in the global market for the supply of photonic chip simulation software.

(186) The results of the market investigation provide evidence that the Parties are competing. In particular, a majority of customers of optics software who expressed a view during the Commission's market investigation consider that when deciding which software to use, customers mostly weigh Synopsys' tools OptSim with Ansys' tool Lumerical Interconnect (and vice-versa).[175]

(187) This view is also shared by the Parties' customers, as one explains that "*Synopsys and Ansys do indeed compete closely in the field of photonic chip simulation tools, as both companies offer advanced solutions that cater to the growing need for photonic design, simulation, and verification. While there are some differences in their approaches and specific tool capabilities, both Synopsys and Ansys provide comprehensive photonic design suites and have established themselves as leaders in the field*".[176]

(188) In addition, one internal document of Ansys suggests that the Parties treat each other as benchmark competitors against whom they measure their performance.[177] The document entitled *"*[…]*"* compares some Synopsys' and Ansys' tools, including OptSim and Lumerical Interconnect. The [document] assesses their [Ansys' assessment of relevant product attributes].

(189) In the second place, the Commission considers that the Merged Entity will continue to face sufficient competitive constraints post-Transaction. This applies when considering competition both from all kinds of providers but also from purpose-built photonic chip simulator providers only.

(190) *Firstly*, Ansys and Synopsys will face competition from at least eight competitors, including purpose-built photonic chip simulator providers, such as VPI Photonics ([10-20]%), Optiwave Systems ([0-5]%), Photon Design ([0-5]%), as well as electrical circuit simulator providers, such as Cadence ([30-40]%), Keysight ([10-20]%), Empyrean ([5-10]%) and Siemens ([5-10]%).

(191) With respect to electrical circuit simulators, the Notifying Party submits that **Cadence**'s tool Spectre, **Keysight**'s tool PathWave ADS, **Siemens**' tool AFS[178] and **Empyrean**'s tool ALPS, which are originally conceived for electronic chips, can also be used for photonic chip simulation. Synopsys' tool PrimeSim could also be used for photonic chip simulation, [product use information].

(192) Synopsys' internal documents confirm that customers use an electrical circuit simulator for photonic chip simulation. For example, in an internal correspondence [engagement with customers on product features].[179] In another document [engagement with customers on product features].[180]

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175 Replies to Questionnaire to users and providers of optics and photonics software, question E.3.

176 Market participant's response to the CMA's RFI of 21 October, question 22.

177 Ansys internal document, ANNEX 5.4(C)(ANSS), […], April 2022".

178 See https://eda.sw.siemens.com/en-US/ic/analog-fastspice/.

179 Parties' response to the European Commission's RFI 25, Annex RFI 25 Q 3.1.

180 Parties' response to the European Commission's RFI 25, Annex RFI 25 Q 3.3.

(193) This is also evidenced by a foundry testimonial, which confirms that they "*currently support customers in simulating photonic chips using an electrical simulator with a Verilog-A model*" and considers that "*Given the install-base of electronic simulators and the growing complexity of photonic designs, one could assume that the trend of simulating photonic devices with electronic simulators will grow over the next five years*".[181] One competitor of the Parties also shared this view that the global market of the supply of photonic chip simulation software is growing: "*Demand for photonic design tools, including photonic design implementation and photonic chip simulation tools, is expected to grow substantially in the next five years*".[182]

(194) In addition, the results of the market investigation confirm the use of electrical circuit simulators. Cadence and Siemens are both mentioned as alternative providers to Synopsys and Ansys for photonic chip simulation by several customers.[183]

(195) *Secondly*, even if electrical circuit simulators were not to be considered as an alternative to purpose-built photonic chip simulators, the Merged Entity will still face sufficient competitive constraints post Transaction.[184]

(196) As mentioned above, several players offer dedicated photonic chip simulators which compete with the Parties' tools.[185]

(197) **VPIphotonics**, headquartered in Germany, offers a photonic chip simulation tool VPIcomponentMaker and a fibre-optic communication system simulator VPItransmissionMaker. VPIphotonics' tools interoperate with Keysight' and Siemens' layout design implementation tools.[186]

(198) **Optiwave Systems**, headquartered in Canada, offers a suite of photonics and photonic chip software. Its OptiSPICE tool is used for photonic and electric circuit simulation and has c. 15,000 users across its photonic software solutions.[187]

(199) **Photon Design**, headquartered in the UK, offers the photonic chip simulation tool PICWave. Photon Design's solutions are "*in use in 30+ countries, 100s of research labs and contributed to 1000s of leading research publications*".[188]

(200) The customers who expressed a view in the Commission's market investigation consider that there are several meaningful alternative providers to Synopsys and Ansys. As pointed out by two customers, "*to design and simulate photonic chips*

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181 Market participant's response to the CMA's RFI on photonic chip simulation, 3 Decembre 2024.
182 Market participant's response to the CMA's RFI of 21 October, question 22.
183 Replies to Questionnaire to users and providers of optics and photonics software, question E.1.
184 As relevant EDA markets are closed at the functional level for the purpose of this Decision (see Section 4.2.1.4), it is not appropriate to further segment EDA functions according to the type of chip. This holds in particular for electronic design tools for analog chips and purpose-build tools for photonic chips serving the same EDA function.
185 Conservatively excluding electrical circuit simulators from the photonic chip simulation market (quod non) and assuming that the offers of Cadence, Siemens, Keysight and Empyrean are exclusively considered electrical circuit simulators and excluding these competitors from the photonic chip simulation market, the remaining competitors VPIphotonics, Optiwave Systems and Photon Design would have market shares of [20-30]%, [5-10]% and [5-10]% respectively (based on 2023 data).
186 See www.vpiphotonics.com/Tools/PhotonicCircuits/.
187 See optiwave.com/.
188 See www.photond.com/company.htm.

we also consider VPI" which *"is generally on the same level for circuit level simulation or even more advanced than Ansys Lumerical Interconnect*."[189] Latitude Design Systems and Luceda Photonics are also mentioned by several customers in response to the market investigation as constituting an alternative to the Parties' tools for photonic chip simulation.[190] In that sense, one customer also shared that "*For European project, we are encouraged to collaborate with other software providers like Luceda or VPIphotonics*".[191]

(201) In addition, the majority of customers who expressed a view in the Commission's market investigation considered it likely that new providers could launch a competitive product within the next two years.[192] As example of recent entry, customers mentioned Latitude Design Systems, already cited by the Notifying Party and considered above as a credible alternative by other respondents to the market investigation, and Flex Compute. In this respect, customers explain that:

- "*Latitude is another new provider that we would consider more for circuit level simulations and photonic chip design, and Flex Compute which offers a very interesting photonic FDTD simulation tool, mostly for passive photonic structures*".

- "*FlexCompute is a recent entry for photonics software*"

- "*There are more alternative tools and service providers with decent expertise in photonics and hence they may come up to the market with similar solutions as ANSYS and Synopsys*"

- "*These areas are fairly new, not very mature and have always been experimental. Therefore, [customer] believes that it is possible for new players to enter the market in the next two years*"[193]

(202) On this basis, the Commission considers that the global market for the supply of photonic chip simulation software is dynamic, characterised by a variety of providers, including recent players such Latitude Design Systems. Given that this market is growing, it cannot be excluded that other players will enter the market for the supply of photonic chip simulation software in the coming years.

5.3.2.3.3. Conclusion

(203) In view of the above considerations and in light of the results of the market investigation and the evidence and information available to it, the Commission concludes that the Transaction does not raise serious doubts as to its compatibility with the internal market resulting from horizontal non-coordinated effects on the global market for the supply of photonic chip simulation software.

5.3.2.4. Global market for the supply of RTL Power consumption analysis

(204) Power consumption analysis checks the power specification of a digital chip, i.e., how much power it consumes and thus requires to function.

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189 Replies to Questionnaire to users and providers of optics and photonics software, question E.4.
190 Replies to Questionnaire to users and providers of optics and photonics software, question E.1.
191 Replies to Questionnaire to users and providers of optics and photonics software, question E.4.
192 Replies to Questionnaire to users and providers of optics and photonics software, question E.11.
193 Replies to Questionnaire to users and providers of optics and photonics software, question E.12.

(205) Power consumption analysis is carried out at two levels: RTL level - early stage of the design process (architectural design), where designs go through many modifications and speed is the key, and gate-level - later stage of the design flow (logic/circuit design), when accuracy is more important.

(206) Both Parties offer RTL power consumption analysis tools (Synopsys offers PrimePower RTL and SpyGlass Power, and Ansys offers PowerArtist), which are assessed below.[194]

5.3.2.4.1. The Notifying Party's view

(207) The Notifying Party submits that the Transaction will not raise competition concerns in the global market for the supply of RTL power consumption analysis tools.[195]

(208) **First**, the Notifying Party considers that the Parties do not compete closely, as their tools have distinct focuses and are based on different technologies. The Notifying Party described as follow the differences between their tools:

- **Synopsys' PrimePower RTL** is used for analyses that require high levels of accuracy. This is particularly valued for fine-grained analysis of power-performance trade-offs for applications, such as chip-level power prediction, and thermal and power grid planning. However, PrimePower RTL has a slower runtime. It is based on fast, physical synthesis technologies, with awareness of timing constraints and physical effects.

- **Synopsys' SpyGlass** is an older product similar to PrimePower RTL, used for lower accuracy RTL analyses at medium speed, such as examining large sources of wasted power, and evaluating alternative designs for lower power consumption. It is based on fast, non-physical synthesis technologies (logical synthesis).

- **Ansys' PowerArtist** is used for general purpose RTL power analysis enabling RTL designers and power methodology engineers to improve the power efficiency of their RTL code. It is based on logic inferencing technologies, which allows considerably faster, but less accurate analysis. It is therefore useful for early analysis, such as rapid power profiling, where speed is key. PowerArtist also has an advanced Graphical User Interface ("GUI"), which help RTL designers unfamiliar with power analysis to enable them to be more productive in the design process.

(209) **Second**, the Notifying Party submits that, even if Synopsys and Ansys broadly compete for the same customers i.e., customers seeking an RTL power consumption analysis tool, they do not have the same customers. In Ansys' experience, certain customers can and do purchase both tools but for different use cases.

(210) In addition, Synopsys' competitive displacement data for 2023 records [sales information]. [Sales information], which shows that the client did not consider

194 In gate-level power consumption analysis, Synopsys offers PrimePower. Ansys' gate-level power consumption analysis tool (PowerArtist-SC) [Ansys' product sales].

195 Form CO, paragraphs 386, and seq.

Synopsys' tools to offer a strong competitive alternative in the Notifying Party' view.

(211) Therefore, the Notifying Party considers that the displacement data is consistent with the lack of close competition between PowerArtist and PrimePower RTL or SpyGlass Power.

(212) **Third**, the Notifying Party considers that the Merged Entity will continue to face significant competition from two other competitors, Cadence and Siemens:

- Cadence's Joules RTL has been introduced more recently, but it has been growing rapidly. It is competing closely with both Synopsys' PrimePower RTL and SpyGlass Power and Ansys' PowerArtist, as it is able to offer (i) higher accuracy of results (similar to PrimePower RTL and SpyGlass Power) at (ii) a greater speed (similar to PowerArtist). Cadence has improved Joules' RTL power reduction capability and run time performance and now performs better than Synopsys' tools in these capabilities. In addition, Cadence has improved Joules' GUI or user environment, and it is better than Synopsys' tools in this capability.

- Siemens' Power Pro**,** which has been sold for over 10 years, provides high accuracy as it also takes account of physical effects. It is particularly distinguished by its ability to generate RTL code that is power-optimised, offering "automatic RTL power reduction". Ansys views Siemens' PowerPro as the closest competitor to PowerArtist. This is because PowerPro provides similar capabilities to PowerArtist for the primary use cases in RTL Power Consumption Analysis, including power consumption analysis, generating power metrics, and power reduction analysis, with features such as "stability and observability techniques" and "automatic RTL re-write". Synopsys considers PowerPro a versatile RTL Power Consumption Analysis tool that can provide fast analysis with an appropriate level of accuracy for most use cases.

(213) **Fourth**, the Notifying Party submits that the Parties' solutions are complementary and could give rise to efficiencies post-Transaction. In that regard, Synopsys and Ansys have formed multiple working groups with product and R&D leaders from both companies, supported by the consulting firm Deloitte, to refine post-transaction opportunities to develop new joint solutions. [Synopsys' product development plans].[196]

5.3.2.4.2. The Commission's assessment

(214) The Commission considers that the Transaction raises serious doubts as to its compatibility with the internal market on the global market for the supply of RTL power consumption analysis, resulting from horizontal non-coordinated effects.

(215) This is because (i) the Parties' combined market share is high and the increment as a result of the Transaction is significant (Section 5.3.2.4.2.1), (ii) the Parties are

[196] Form CO, paragraphs 404. See also the August 22, 2024 interim report (the "New Joint Solutions Plan") annexed as Exhibit A to the FTC Efficiencies Paper (Chapter 2 – Annex 7) that describes the current status in the development of those plans. Responsive to Q.14 of PN RFI 15.

close competitors (Section 5.3.2.4.2.2) (iii) competitive constraints from the two remaining competitors are insufficient (Section 5.3.2.4.2.3.). In addition, the Commission considers that the reduction of the competitive pressure resulting from the Transaction is not likely to be outweighed by other competitive constraints such as potential entry.

5.3.2.4.2.1. The Parties' combined market share is high and the increment is significant

(216) As set out in the Horizontal Merger Guidelines, market shares and concentration levels provide useful indications of the market structure and of the competitive importance of both the merging parties and their competitors.

(217) Based on share data provided by the Parties, as set out in Section 5.2 above, in the market for the supply of RTL power consumption analysis, the Merged Entity would have a share of [70-80]% in 2023 (table 3 above). The increment in market share would also be significant (accounting for [30-40]%), as the Parties […]. The Commission also notes that both Parties' shares have been steadily growing over the last three years (combined increased by [5-10] percentage points from 2021 to 2023).

(218) The Commission considers that the market share of the Merged Entity would be substantial and reveal its competitive importance. In fact, the Transaction would create a clear new market leader on the worldwide market for the supply of RTL power consumption analysis, with Siemens and Cadence, the second and third players in the market, being much smaller than the Merged Entity, with respectively [10-20]% and [10-20]%.

5.3.2.4.2.2. The Parties are close competitors

(219) The Commission considers, contrary to the Notifying Party' argument set out in Section 5.3.2.3.1 above, that the Parties are close competitors, based on a number of elements.

(220) **First**, when asked whether PowerArtist (Ansys) competes with PrimePower RTL (Synopsys), most of the respondents to the Commission's market investigation considered the Parties' tools to be competing closely.

(221) All competitors that expressed a view in the Commission's market investigation indicated that the Parties' tools compete closely. As summarised by one competitor of the Parties, "*Both Synopsys' PrimePower RTL and Ansys' PowerArtist are widely recognized tools in the domain of RTL power consumption analysis. They offer overlapping functionalities, such as: Power estimation and optimization at the RTL level. Early-stage power analysis to guide architectural and design decisions. Energy-saving measures through power profiling and debug capabilities. Both tools cater to design teams focusing on early-stage power analysis. While the tools have their unique strengths (e.g., PowerArtist's user-friendly interface vs. PrimePower RTL's seamless Synopsys flow integration), their core functionalities overlap significantly. Customers may compare these tools directly when selecting RTL power analysis solutions*".[197]

[197] Replies to Questionnaire to customers of EDA and design IP, question D.A.A.6.1.

(222) PrimePower RTL and PowerArtist are also the main tools considered by customers when they want to carry RTL power consumption analysis. While some customers acknowledged that the features of the Parties' tools are different – highlighting also the fact that PrimePower RTL is more accurate – the majority of customers that expressed a view in the market investigation considered that the Parties' tools compete closely.[198] For instance, one customer explained that, even if their "*features are slightly different*", the Parties compete closely as "*Power Artist and Prime Power RTL are used to analyze and optimize power consumption for an electronic design at the front end RTL (Register Transfer Level) stage*."[199]

(223) **Second**, some internal documents of the Parties suggest that the Parties compare their tool to that of the other Party, as well as of other competitors.

(224) One Synopsys' internal document dated August 2022 describes the competitive landscape in "Power" – including RTL power competitive analysis – and compares its tools and those of its competitors in power analysis[200]. [Synopsys competitive assessment of tools].

Figure 6: Synopsys' presentation of the competitive landscape in the market of the supply of RTL power consumption analysis

[…]

Source: Synopsys internal document, […], August 2022.

(225) A similar observation can be made with the Synopsys' self-assessment document below, that compares its performance with Ansys' and [Competitor's] tools. This internal document quoted by the Parties shows that, [Synopsys' competitive assessment of tools].[201]

Figure 7: Synopsys' self-assessment of the strengths and weaknesses of vendors' RTL power analysis tools

[…]

Source: Form CO, paragraph 390

(226) **Third**, the Commission has gathered evidence showing that Synopsys and Ansys' RTL power consumption analysis tools compete for the same customers.

(227) <u>In the first place</u>, some Synopsys' internal documents contain information on customers displacements […].[202].[203]

(228) <u>In the second place</u>, the Notifying Party indicated in the Form CO that one customer, [Synopsys' customers' practices in evaluating tool options and

198 Replies to Questionnaire to customers of EDA and design IP, question D.A.A.6.
199 Replies to Questionnaire to customers of EDA and design IP, question D.A.A.6.1.
200 Synopsys internal document, […], August 2022.
201 Form CO, paragraph 390.
202 Synopsys internal document, […].
203 Synopsys internal document, […], dated 13 April 2021.

comparing tools from various providers]. This illustrates that when customers are looking for a RTL power consumption analysis provider, they consider both Synopsys and Ansys offerings.

(229) In addition, the Notifying Party submits that, in Ansys' experience, certain customers can and do purchase both tools of the Parties[204], which imply that Synopsys and Ansys' RTL power consumption analysis tools compete for the same customers.

(230) The Commission notes that the above evidence offsets the displacement data submitted by the Notifying Party in the Form CO aimed at establishing that the Parties do not compete for the same customers.

5.3.2.4.2.3. Customers have limited possibilities of switching to other suppliers

(231) The Horizontal Merger Guidelines provide, at paragraph 31, that where customers of the merging partes may have difficulties switching to other suppliers because there are few alternative suppliers, such customers are particularly vulnerable to price increases.

(232) The Commission considers that in the present case customers will retain limited possibilities of switching to other suppliers post-Transaction for the reasons outlined below.

(233) **First**, the results of the market investigation reveal that the majority of customers considered that PrimePower RTL (Synopsys) is the main alternative to Power Artist (Ansys) and vice versa[205]. Therefore, according to Parties' customers, when they change supplier, they prefer the other Party to Cadence or Siemens.

(234) **Second**, the Transaction would leave customers with two other suppliers of RTL power consumption analysis competing with the Merged Entity, Cadence and Siemens. As it is explained below, the results of the market investigation show that these alternatives are not as appealing as the Synopsys' and Ansys' offering.

(235) In the first place, the Notifying Party indicated that Siemens' PowerPro is a well-established tool with unique features, which has been sold for over 10 years.[206]

(236) Although PowerPro has been ranked as being similar in quality to the Parties' tools by the customers which responded to the market investigation,[207] the results of the market investigation also provide evidence that Siemens's tool does not seem to be a good alternative to the Parties' tools. Customers contacted during the preliminary market investigation estimated that:

(a) "*Siemens' tool PowerPro is not convincing*" and

(b) "*[it] does not view currently PowerPro by Siemens as a feasible alternative. However, it could be developed into a comparable tool in 5-10 years, with sufficient R&D investments*".[208]

204 Form CO, paragraph 388.
205 Replies to Questionnaire to customers of EDA and design IP, questions D.A.A.2 and D.A.A.3.
206 Form CO, paragraph 401.
207 Replies to Questionnaire to customers of EDA and design IP, question D.A.A.4.
208 Minutes of a call with a market participant dated 23 July 2024, para. 7.

(237) The Commission notes that this is consistent with Siemens' market position based on its market share. Siemens holds [10-20]% share in 2023, which is […] smaller than the Merged Entity's market share post-Transaction. In addition, between 2021 and 2023, Siemens has lost shares ([0-5]% percentage points). This confirms that, in the recent years, customers have decided not to select Siemens' offer in their choice of RTL power consumption analysis providers.

(238) In the second place, the Parties indicated that Cadence's *Joules RTL* may be described as competing closely with both Synopsys' PrimePower RTL and SpyGlass Power and Ansys' PowerArtist, as it is able to offer (i) higher accuracy of results (similar to PrimePower RTL and SpyGlass Power) at (ii) a greater speed (similar to PowerArtist), Joules RTL.[209]

(239) This is not in line with the views of customers that replied to the market investigation. Customers have ranked Cadence as being inferior to the Parties' tools.[210] The Commission notes that this is consistent with Cadence's share. Joules RTL is currently the smallest competitor in the market for the supply of RTL power consumption analysis, accounting for [10-20]% in 2023. Between 2021 and 2023, Cadence has also lost shares [0-5]%.

(240) **Fourth**, customers also indicated that switching EDA vendors is cumbersome. In that regard, two customers of the Parties consider that switching is "*very expensive and time-consuming*" and "*is difficult to realize in the short term (learning curve, impact on projects, impact on legacy designs). Overall, switching requires months to years depending on the type of tools*".[211] This proves that even if there are alternatives to the Parties, it is difficult in practice to change providers.

(241) **Fifth,** the results of the market investigation have not provided concrete evidence of alternative providers that will compete with the Parties in the near future. The Commission considers that any potential entrants on the market for RTL power consumption analysis would face significant barriers to entry. Any threat to entry would not be sufficiently likely, strong and timely.

(242) In the first place, the Commission notes that the Notifying Party has not mentioned recent entrants or the existence of low barriers for a new provider to enter the market of supply RTL power consumption analysis in the Form CO.

(243) In the second place, this is consistent with the results of the market investigation. While some respondents indicated that future entry would be possible in the market for the supply of RTL power consumption analysis, most of the respondents which shared their view consider unlikely that a new provider could launch a competitive power consumption analysis product within the next two years.[212] In that regard, customers indicated that:

(a) *"[Customer] does not consider it likely that a new provider could launch a competitive power consumption analysis product within the next two years because it is unlikely that any new EDA tool in any space could be launched in such a short period of time and be competitive with existing, established tools*."

209 Form CO, paragraph 401.
210 Replies to Questionnaire to customers of EDA and design IP, question D.A.A.4.
211 Replies to Questionnaire to customers of EDA and design IP, question C.A.6.
212 Replies to Questionnaire to customers of EDA and design IP, question D.A.A.7.

(b) *"Seems hard, given that you need to correlate these tools with silicon results, which is very expensive"*

(c) *"Unlikely a start-up would introduce a new tool in such a competitive landscape."*[213]

(244) In addition, as highlighted by some respondents to the Commission's market investigation, potential entrants may encounter high barriers to enter the market for RTL power consumption analysis, since it would take for a new provider "*multiple years to adopt any new technology"*.[214]

5.3.2.4.3. Conclusion

(245) In view of the above considerations and in light of the results of the market investigation and the evidence and information available to it, the Commission concludes that the Transaction raises serious doubts as to its compatibility with the internal market resulting from horizontal non-coordinated effects on the global market for the supply of RTL power consumption analysis.

5.3.2.5. Global market for the supply of transistor-level power integrity analysis

(246) Power integrity analysis checks a chip's reliability when using power, to ensure it will continue to function correctly. This includes checking that the chip will not succumb to electromigration ("EM") or a drop in voltage ("IR"). This analysis is typically done at the final stage of the chip design flow (the sign-off stage) to ensure that the chip meets foundry requirements.[215]

(247) Power integrity is run at transistor-level for both analog and custom chip design, and at gate-level for digital chip design, each requiring different tools. In the case multi-die chips, the level of analysis and respective tool used will vary depending on the type of chiplet (either digital or analog), while mixed-signal chip design will require both types of analysis. The Parties' activities horizontally overlap with regards to transistor-level power integrity analysis tools, where Synopsys offers PrimeSim Reliability Analysis ("PrimeSim RA") and Ansys offers Totem(-SC). [216]

5.3.2.5.1. The Notifying Party's view

(248) The Notifying Party submits that the Transaction only gives rise to a small increment and will not significantly impede competition for the supply of transistor-level power integrity tools, for the following reasons.

(249) **First**, the Parties are not close competitors as their tools have primarily different technical capabilities, and differ significantly in functions, performance, customers, and use cases. PrimeSim RA focuses on reliability and robustness analysis, whereas Totem focuses specifically on transistor-level power integrity analysis.[217] The Notifying Party submits that PrimeSim RA lacks advanced features required to compete effectively with Totem in transistor-level power integrity analysis, namely

213 Replies to Questionnaire to customers of EDA and design IP, question D.A.A.7.1.
214 Replies to Questionnaire to customers of EDA and design IP, question D.A.A.7.1.
215 Form CO, para. 405 and 406.
216 Form CO, para. 405 and 406.
217 Form CO, para. 420. Parties' response to the European Commission's RFI 25, para. 1.17.

static or hierarchical analysis capabilities, which are crucial in the case of large and complex chip designs.[218]

(250) In addition, the customers of transistor-level power integrity analysis in PrimeSim RA use it for very niche cases, like the verification of library cells, as extension to circuit simulators, whereas Totem is widely used for transistor-level power integrity tool in interactive flows for analog circuits.[219]

(251) **Second**, the Merged Entity will continue to face strong competition from segment leader Cadence, and recent entrants including Siemens and Empyrean, who the Parties expect to grow further.[220]

(252) Cadence (Voltus-XFi) pioneered transistor-level power analysis solutions and is the historic leader in this function with a c. [40-50]% global share. Cadence is the preferred vendor for many leading customers (e.g., […] and […]), and [sales information] in some [sales information] accounts in recent years.[221]

(253) Siemens' mPower Analog, an award-winning solution, which was launched in 2021, has quickly gained traction and market share and has already received certification for use in digital and/or analog designs from TSMC, from GlobalFoundries and with Tower Semiconductor. Siemens is currently aiming to certify mPower Analog at Samsung Foundries.[222]

(254) Empyrean's Patron is a successful and fast-growing new entrant. Empyrean is a Chinese company that has been making headway in power integrity analysis and launched Patron in 2022. Empyrean claims that Patron's features run "2 times faster than traditional tools" and balances the speed-accuracy tradeoff by offering two modes, one focusing on fast turnaround and the other focusing on providing high accuracy. It also competes very aggressively on price.[223]

5.3.2.5.2. The Commission's assessment

(255) The Commission considers that Transaction does not raise serious doubts as to its compatibility with the internal market in the global market for the supply of transistor-level power integrity analysis, resulting from horizontal non-coordinated effects.

(256) This is because (i) the increment resulting from the Transaction is small (Section 5.3.2.5.2.1.), (ii) while the Parties are viewed as two of the few alternatives in a concentrated market, close competition between the Parties has not been confirmed (Section 5.3.2.5.2.2.); and (iii) the Parties will continue to face significant competitive constraints (Section 5.3.2.5.2.3.).

5.3.2.5.2.1. The increment resulting from the Transaction is small

(257) The Commission notes that the Transaction would give rise to a combined market share [40-50]% in global market for transistor-level power integrity analysis (see

218 Parties' response to the European Commission's RFI 25, para. 1.18.
219 Parties' response to the European Commission's RFI 25, para. 1.18
220 Form CO, para. 422.
221 Form CO, para. 422. Parties' response to the European Commission's RFI 25, para. 1.4.
222 Form CO, para. 422. Parties' response to the European Commission's RFI 25, para. 1.5.
223 Form CO, para. 422. Parties' response to the European Commission's RFI 25, para. 1.14.

Table 6 above). However, the increment coming Synopsys is very small (i.e. [0-5]%) which is explained by the fact that Synopsys' PrimeSim RA is a broader purpose tool for reliability and robustness analysis and, therefore, according to the Notifying Party's estimates, , out of PrimeSim RA's USD […] global revenues in 2023, only USD […] are related to usage for transistor-level power integrity, out of which only USD […] were made in the EU.[224]

5.3.2.5.2.2. The Commission's investigation has not confirmed that the Parties would be close competitors

(258) The Commission considers that, while the Parties are considered as two of the only few alternatives in the market, namely in view of the high level of concentration, the Parties tools appear to have different focuses and the Transaction does not raise concerns from customers or competitors due to reduction of alternatives in this market.

(259) **First**, the results of the market investigation indicated that Cadence's Voltus-XFi is the closest alternative to both Ansys' Totem-(SC) and Synopsys' PrimeSim RA but the Parties' tools are still viewed as alternatives.

(260) The majority of respondents to the market investigation who expressed a view considered Voltus-XFi as an alternative to Totem(-SC), while Synopsys' PrimeSime RA and Siemens' mPower Analog were, respectively, the second and third most chosen options.[225] A very limited number of respondents considered Empyrean's Patron as an alternative.[226] With regards to alternatives to PrimeSim RA for transistor-level power integrity, the results of the market investigation were inconclusive, as the majority of respondents replied "I don't know", the second most chosen option being Voltus-XFi.[227]

(261) In addition, when asked to rate the strength/quality of the tools below for transistor-level power integrity analysis, the majority of respondents who expressed a view rated Totem(-SC) as the best tool, followed by Voltus-XFi and PrimeSim RA.[228] Both mPower Analog and Patron received lower ratings.[229]

(262) **Second**, the results of the market investigation were inconclusive on whether the Parties compete closely. Even though the Parties' tools were considered as two of the few alternatives in a concentrated market, when asked whether the Parties' tools "serve distinct purposes and compete loosely" or "compete closely", the majority of respondents replied "I don't know".[230]

(263) Nonetheless, customers have confirmed the Parties' claims with regard to the different focus and uses of the tools:

(a) "*We do not consider that Synopsys and Ansys compete closely in the supply of transistor-level power integrity tools* […] *The field of use for both tools are different as Anysys' Totem/Totem-SC is used to analyse power*

224 Parties' response to the European Commission's RFI 25, para. 1.17.
225 Replies to Questionnaire to customers of EDA and design IP, question D.A.D.1.
226 Replies to Questionnaire to customers of EDA and design IP, question D.A.D.1.
227 Replies to Questionnaire to customers of EDA and design IP, question D.A.D.2.
228 Replies to Questionnaire to customers of EDA and design IP, question D.A.D.3.
229 Replies to Questionnaire to customers of EDA and design IP, question D.A.D.3.
230 Replies to Questionnaire to customers of EDA and design IP, question D.A.D.5.

characteristics by checking weak characteristics in the layout while Synopsys' PrimeSim-EMIR is used to check circuit operation by power."[231]

(b) "*In contexts where both tools are used for power integrity analysis, they may overlap. Both can handle aspects of power integrity, but they do so with different strengths and focuses, leading to competition in certain scenarios.*" / "*While both tools have overlapping capabilities in power integrity analysis, they have distinct primary purposes: PrimeSim RA focuses on mixed-signal simulation, while Totem(-SC) is dedicated to power integrity. The choice between them should be based on the specific needs of the design, whether that be mixed-signal interactions or in-depth power integrity analysis.";*[232]

(c) "*These tools have different functionalities and purposes*";[233]

(d) "*Synopsys PrimeSim RA can be used for reliability simulations while Totem-SC is primarily used for EMIR.*";[234]

(e) "*Ansys Totem-SC analyzes transistor level power noise and reliability for analog mixed-signal designs including power integrity, substrate noise, and EM analysis. PrimeSim RA is used to verify the reliability of ICs throughout their lifecycle and provides reliability analysis including electromigration/IR drop analysis, design robustness, MOS aging, analog fault simulation, and circuit checks (ERC) to enable full-lifecycle reliability verification.*".[235]

(264) In addition, some customers also highlighted certain unique features of Totem(-SC):

(a) "*Totem SC is the only tool we know with effective gate level power models. Totem SC is also uniquely compatible with technology exploration and development of novel transistor technologies.*";[236]

(b) "*Our requirements to support a broad swathe of technology nodes is only satisfied by Totem. All the other tools suffer from non-convergence or limited technology support*";[237]

(c) "*Efficiently handles large-scale designs with billions of transistors / Delivers fast turnaround time for analysis and optimization / Accurately models complex physical phenomena, such as electromigration, electromechanical stress, and thermal effects / Enables accurate prediction of reliability issues / Supports a wide range of analysis types, including IR drop, EM interference, thermal analysis, and reliability analysis.*";[238]

(d) "*Totem(-SC) is unique because it provides detailed power integrity analysis at the transistor level, particularly for mixed-signal and multi-die chips. Its graphical user interface and ability to integrate seamlessly with other EDA tools make it a preferred choice for analyzing complex designs.*"[239]

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231 Replies to Questionnaire to users and providers of EDA and design IP, question D.A.D.4.
232 Replies to Questionnaire to customers of EDA and design IP, question D.A.D.5.1.
233 Replies to Questionnaire to customers of EDA and design IP, question D.A.D.5.1.
234 Replies to Questionnaire to customers of EDA and design IP, question D.A.D.5.1.
235 Replies to Questionnaire to customers of EDA and design IP, question D.A.D.5.1.
236 Replies to Questionnaire to customers of EDA and design IP, question D.A.D.4.
237 Replies to Questionnaire to customers of EDA and design IP, question D.A.D.4.
238 Replies to Questionnaire to customers of EDA and design IP, question D.A.D.4.
239 Replies to Questionnaire to customers of EDA and design IP, question D.A.D.4.

(265) **Third,** the results of the market investigation indicated that the Transaction will likely not have a negative impact in the market for transistor-level power integrity.

(266) The majority of respondents who expressed a view considered that the Transaction would have a "neutral" impact in the market for transistor-level power integrity, while almost one third replied that the impact would be "positive".[240] In this sense, customers generally highlighted that the Transaction could lead to more innovation and that, in any case, there will still be viable alternatives in the market. For instance:

(a) "*The transaction could foster innovation and improved methodologies in transistor-level analysis, enhancing the overall performance of these tools.*";[241]

(b) "*EDA customers will continue to benefit from competition from Cadence and other suppliers.*";[242]

(c) "We also think this [Transaction] could speed innovation in new technology enablement".[243]

(267) Finally, it should be noted that none of the customers or competitors of the Parties have expressed any specific concerns with regards the market for transistor-level power integrity.

(268) Accordingly, while there may be some level of competition between the Parties' tools for the capabilities in which there is an overlap, the Commission considers that close competition has not been confirmed by the results of the market investigation.

5.3.2.5.2.3. The Merged Entity will continue to face sufficient competitive constraints

(269) The Commission considers that the Merged Entity will continue to face sufficient competitive constraints coming from Cadence and recent entrants, in particular Siemens, which will likely increase its market position.

(270) **First**, Cadence will continue to exert significant competitive pressure with its tool Voltus-XFi, which has been historically the market leader and currently has [40-50]% market share (see Table 4 above).

(271) Voltus-XFi benefits from integration with Cadence's Virtuoso chip design platform and works smoothly with other Cadence tools, such as its simulator, Spectre, to achieve a faster design flow, being certified by several major foundries and offering comparable advanced features.[244] As evidenced by the results of the market investigation, Voltus-XFi competes closely with Totem(-SC) as it was considered the best alternative to Totem(-SC) and received the highest rating of strength/quality of the tool, after Totem(-SC).[245] As indicated by one respondent to the market investigation, "*Ansys Totem and Cadence Voltus-XFi both provide*

240 Replies to Questionnaire to customers of EDA and design IP, question E.3.
241 Replies to Questionnaire to customers of EDA and design IP, question E.3.1.
242 Replies to Questionnaire to customers of EDA and design IP, question E.3.1.
243 Replies to Questionnaire to customers of EDA and design IP, question E.3.1.
244 Form CO, para. 422.
245 Replies to Questionnaire to customers of EDA and design IP, question D.A.D.1 and D.A.D.3.

leading edge EMIR verification solutions with a good support by mature node and small node SC foundries.".[246]

(272) Ansys' internal documents report Voltus-XFi as one of the segment's biggest players with the most positive attributes.[247] For instance, one internal document states that "[Ansys' market intelligence on its competitors].". Another Ansys' internal document highlights that [Ansys' market intelligence on its competitors]".[248]

(273) An Ansys internal email exchange [Ansys' market intelligence on its competitors].[249]

(274) Voltus-XFi is also the preferred vendor for many leading customers (e.g., [Ansys' customer] and [Ansys' customer]), and [sales information] in some [sales information] accounts in recent years (e.g., [Ansys' customers]).[250]

(275) **Second**, the Merged Entity will face incremental competitive pressure from recent entrants, particularly Siemens' mPower Analog.

(276) In the first place, even though mPower Analog was only launched in September 2021, it has already received certification for use in digital and/or analog designs from three foundries and is quickly gaining market traction, having already a higher market share than Synopsys' PrimeSim RA, with [5-10]% in 2023. As explained above, the results of the market investigation showed that mPower Analog is already perceived as an alternative by some of the market respondents who expressed a view.[251]

(277) In addition, mPower Analog's market position is expected to grow, given its technical capabilities and competitive advantages. In particular, Siemens' tool can be deployed across both analog and digital designs, which means that customers designing both types of chips, mixed-signal chips or multi-die chips, which combine both analog and digital element, can rely on the same tool. Therefore, mPower Analog is well positioned to become more prevalent with the growing use of Internet of Things ("IoT") devices and multi-die chips. Furthermore, mPower Analog's performance is built on the hierarchical analysis technologies of Siemens' leading physical verification tool Calibre.[252]

(278) In the second place, the Parties' internal documents show mPower Analog is a competitive tool. [Ansys' customers' preferences and internal market intelligence on its competitors]. For instance:

(a) [Ansys' customers' preferences].[253]

(b) [Ansys' customers' preferences].[254]

(c) [Ansys' market intelligence on its competitors].[255]

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246 Replies to Questionnaire to users and providers of EDA and design IP, question D.A.D.4.
247 Parties' response to the European Commission's RFI 25, para. 1.4.
248 Ansys' internal document, Annex 5.4(c)(ANSS), […].
249 Ansys' internal document, Annex RFI 25 Q1.4..
250 Parties' response to the European Commission's RFI 25, para. 1.4.
251 Replies to Questionnaire to customers of EDA and design IP, question D.A.D.1. and D.A.D.2.
252 Parties' response to the European Commission's RFI 25, para. 1.7.
253 Ansys' internal document, Annex PN RFI 25 Q1.2.
254 Ansys' internal document, Annexes PN RFI 14 Q17.1 and Q17.2.

(d) [Ansys' market intelligence on its competitors].[256]

(e) [Ansys' market intelligence on its competitors].[257]

(f) [Ansys' customers' preferences].[258]

(g) [Ansys' market intelligence on its competitors].[259]

(279) Furthermore, as submitted by Ansys, there have been recent examples of [Ansys' customers' preferences]. [260] MaxLinear's usage of mPower is evidenced by a customer testimonial available on Siemens' website, which highlights that "[t]*raditional EM/IR approaches can't handle large analog designs consisting of millions of transistors. The mPower Analog high-capacity dynamic analysis technology enables designers to perform full-chip analog IC design EM/IR analyses that were previously impossible*."[261]

(280) In the third place, the Commission also notes that, while the results of the market investigation have not indicated that Empyrean's Patron is currently a credible alternative – given that only a very small percentage of respondents have considered it as an alternative to either Totem(-SC) or PrimeSim RA – [262] it cannot be excluded that Patron would become a more relevant competitor in the future.

(281) Patron was launched in 2022 and has received certification by International Organization for Standardization (ISO) certification in September 2024. Empyrean claims that Patron's features run "*2 times faster than traditional tools*" and balances the speed-accuracy trade-off by offering two modes, one focusing on fast turnaround and the other focusing on providing high accuracy.[263] The Parties consider Patron [Parties' market intelligence on competitors].[264]

(282) Accordingly, the Commission considers that the Merged Entity would continue to face significant competitive constraints from other market players, in particular from Cadence, the closest competitor to Totem(-SC), and Siemens, which is expected to continue to gain market share in the upcoming years.

5.3.2.5.3. Conclusion

(283) In view of the above considerations and in light of the results of the market investigation and the evidence and information available to it, the Commission concludes that the Transaction does not raise serious doubts as to its compatibility with the internal market as a result of horizontal non-coordinated effects in the market for the global supply of transistor-level power integrity tools.

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255 Ansys' internal document, Annex PN RFI 14 Q18.1.
256 Ansys' internal document, Annex PN RFI 25 Q1.3.
257 Ansys' internal document, Annex 5.4(c)(ANSS) – 022, "[…]".
258 Ansys' internal document, Annex RFI 25 Q1.4.
259 Ansys' internal document, Annex RFI 25 Q1.5.
260 Parties' response to the European Commission's RFI 25, para. 1.13.
261 MaxLinear's customer testimonial, available at Customer Testimonial: Kishore Kathula, MaxLinear | Siemens Software (last access 10 December 2024).
262 Replies to Questionnaire to customers of EDA and design IP, question D.A.D.1. and D.A.D.2.
263 Form CO, para. 422.
264 Form CO, para. 422 and Parties' response to the European Commission's RFI 25, para. 1.15.

5.3.2.6. Global market for the supply of ESD analysis

(284) An Electrostatic discharge ("**ESD**") event is a rapid, spontaneous transfer of electrostatic charge that occurs when two objects at different electrostatic potentials approach one another (e.g., touching a statically charged object and receiving a small spark is an ESD event).

(285) ESD analysis tests for chip failure from the unwanted transfer of static electricity – sometimes resulting in a literal spark – when two objects that have different electric charges come into contact.

(286) In order to assess how a chip responds to or withstands ESD events, ESD tools use different analysis methodologies – namely dynamic[265] or static[266] ESD analysis.

(287) ESD analysis is done both in digital and analog chip design at the physical verification and sign-off stage. Multi-die chip designs also require specialised dynamic ESD capabilities to address the unique complexities of interconnected dies and their packaging, including managing cross-die interactions, distributed discharge paths, and safeguarding sensitive inter-die interfaces.

(288) Synopsys offers two solutions that have ESD capabilities (PrimeESD and IC Validator). Ansys does not provide standalone ESD tools, but offers PathFinder(-SC) as an add-on to Ansys' RedHawk(-SC) and Totem tools.

5.3.2.6.1. The Notifying Party's view

(289) The Notifying Party claims that the Transaction will not give rise to serious doubts as to its compatibility with the internal market for the global market for the supply of ESD analysis, for the following reasons.[267]

(290) **First**, the Parties are not close competitors in the global market for the supply of ESD analysis, as their tools have different areas of focus and distinct customers.

(291) In the Notifying Party' view, Synopsys' PrimeESD is the most advanced ESD analysis tool, competing with other in-depth ESD analysis tools that offer both static and dynamic analysis (such as Siemens' Calibre PERC, Cadence's Voltus ESD or Magwel's ESDi). While Ansys' tool Pathfinder(-SC) offers static analysis capabilities as an add-on functionality rather than a standalone solution.

(292) **Second**, the Parties will continue to face strong competition from various rivals, starting from the segment leader Siemens (Calibre PERC), as well as from Cadence (Voltus ESD), Magwel or Angstrom Design Automation.

(293) With respect to Siemens, the Notifying Party submits that Siemens' Calibre PERC, with [60-70]% share in 2023, is the foundry-certified industry standard and the leading solution in the market for the supply of ESD analysis. It offers static analysis and is more closely comparable to Synopsys' IC Validator. Calibre PERC

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265 Dynamic ESD analysis studies a chip's response to an ESD event over time, which means the way an electrostatic charge behaves over time, including its movement, concentration, and dissipation during an ESD event.

266 Static ESD Analysis looks at how a chip behaves in steady, unchanging conditions, either before or after an ESD event.

267 Form CO, paragraphs 435 and seq.

offers dynamic ESD analysis capabilities through a fully-automated workflow with Solido Simulation Suite.

5.3.2.6.2. The Commission's assessment

(294) The Commission considers that the Transaction does not raise serious doubts as to its compatibility with the internal market in the global market for the supply of ESD analysis for the following reasons.

(295) **First**, the Transaction leads to a moderate combined market share with a limited increment in the global market for the supply of ESD analysis. As shown in table 4 above, in 2023, the Merged Entity's market share was [20-30]%.[268]

(296) According to paragraph 18 of the Horizontal Merger Guidelines, when the market share does not exceed 25%, the concentration "*may be presumed to be compatible with the common market*".[269] As the Commission received specific concerns from one market participant with respect to the market for the supply of ESD analysis, the Commission' market investigation assessed the impact of the Transaction on this market.

(297) **Second**, the results of the Commission' market investigation confirm, even if Synopsys and Ansys are both offering ESD analysis software, the Parties' tools do not compete closely. When asked whether Synopsys' PrimeESD and IC Validator compete with Ansys' PathFinder-SC, most of the Parties' customers considered that the Parties' tools serve distinct purposes. As indicated by one market participant in response to the Commission's market investigation, "*While they all address ESD analysis in some capacity, their specific applications and strengths cater to different aspects of the design process*".[270]

(298) This view is also shared by one competitor of the Parties which indicated that "*While Synopsys' PrimeESD and IC Validator, and Ansys' PathFinder-SC, all provide ESD-related capabilities, they serve distinct purposes and are generally used in complementary or loosely overlapping scenarios*."[271]

(299) **Third**, the Commission considers that post-Transaction there will be enough credible alternatives remaining in the global market of supply of ESD analysis.

(300) Post-Transaction, the Merged Entity will continue to face strong competition from the market leader Siemens (Calibre PERC, [60-70]%), from Cadence (Voltus ESD, [5-10]%), as well as other emerging competitors such as Magwel ([0-5]%).

(301) In addition, the presence of credible alternatives in the global market of supply of ESD analysis is confirmed by the results of the Commission' market investigation.[272] In addition to the competitors cited above, Dassault is also

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268 The Commission notes that the combined market share of the Parties would be higher and above [20-30]% for analog chip and multi-die chip, respectively [20-30]% and [30-40]%.

269 Horizontal Merger Guidelines, para. 18.

270 Replies to Questionnaire to customers of EDA and design IP, question D.A.B.6.1.

271 Replies to Questionnaire to competitor of EDA and design IP, question D.A.B.6.1.

272 Replies to Questionnaire to customers of EDA and design IP, question D.A.B.2.

mentioned by several customers of the market investigation as an alternative to the Parties' tools for ESD analysis.[273]

5.3.2.6.3. Conclusion

(302) In view of the above considerations and in light of the results of the market investigation and the evidence and information available to it, the Commission concludes that the Transaction does not raise serious doubts as to its compatibility with the internal market resulting from horizontal non-coordinated effects on the global market of ESD analysis, even at the most granular level of ESD analysis for multi-die chip.

5.3.2.7. Global market for the supply of power device analysis

(303) Power device analysis tools are used to design and optimise the efficiency and reliability of power devices,[274] like transistors, metal oxide semiconductor field-effect transistors and power management integrated circuits. These tools help to streamline the design process by automating complex simulations that detect and address potential performance bottlenecks, such as electromigration (wear from high current density) and timing inconsistencies, which can impact device reliability. They provide engineers with insights into how to improve layout, reduce power loss, and meet performance and packaging requirements. Generally, power device analysis is run at the physical verification and sign-off stage of analog/custom chip design.[275]

(304) Synopsys offers Power Device Workbench ("PDW"), which is a comprehensive power device analysis tool that is capable of (i) modelling the power devices' overall design from power input to output to identify high resistance areas and evaluate overall efficiency in transmitting power and (ii) analysing gate-level signals in the power device to ensure it turns off and on uniformly for reliability. PDW can be used for all sizes of power devices, as well as with layout tools for analog/custom chip designs.[276]

(305) Ansys' offers PowerX, which performs precise analysis of power devices leveraging specific meshing technology, that allows it to more accurately model and analyse specific areas of a power device design. PowerX does not include layout optimisation functionality.[277]

5.3.2.7.1. The Notifying Party's view

(306) The Notifying Party submits that the Transaction does not give rise to competition concerns in Power Device Analysis.

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273 Replies to Questionnaire to customers of EDA and design IP, questions D.A.B.1, D.A.B.2, and D.A.B.3.

274 Form CO, para. 473. A power device converts electricity delivered from a power outlet into the voltage required by an electronic system. Its function is to ensure sufficient current and voltage are efficiently supplied to a given chip. Power devices are a component of chips composed of one to several transistors (maximum) and must be capable of conducting high levels of current efficiently and without failure (e.g., as a result of overheating).

275 Form CO, para. 474 ad 475.

276 Form CO, para. 476.

277 Form CO, para. 477.

(307) **First**, the Transaction will give rise to a small increment in a in highly-contested market. Ansys had minimal global revenue of $[…] in 2023, representing only [5-10]% in this niche segment (the total size of the Power Device Analysis segment was only $[…] in 2023).[278]

(308) **Second,** the Merged Entity will continue to face strong competition from a wide range of competitors – all but one being stronger than Ansys currently – including Jedat ([20-30]%), Primarius ([10-20]%) (which has acquired Magwel, and Empyrean ([10-20]%). Notably, Empyrean's solution Polas is increasingly being evaluated by many customers due to its improved performance. It will continue to constrain the Merged Entity in this area as a significant competitive force.[279]

5.3.2.7.2. The Commission's assessment

(309) The Commission considers that the Transaction does not raise serious doubts as to its compatibility with the internal market in the global market for the supply of power device analysis tools for the following reasons.

(310) **First**, the Transaction leads to a limited increment in the global market for the supply of power device analysis, as the Parties' combined market share would be [40-50]%, with an increment of [5-10]% coming from Ansys, as shown in Table 7 above.

(311) **Second**, the results of the market investigation were inconclusive on whether the Parties' tools are perceived as close alternatives and compete closely with each other. Some respondents confirmed that Ansys (PowerX) is indeed an alternative to Synopsys (Power Device Workbench), as well as Primarius (PTM), Jedat (PowerVolt) and Empyrean (Polas).[280]

(312) **Third,** the Commission considers that post-Transaction there will be enough credible alternatives remaining in the global market of supply of power device analyis. The Merged Entity will continue to face competition from Jedat ([20-30]%), Primarius ([10-20]%) (which has acquired Magwell), and Empyrean ([10-20]%).

(313) In the first place, Synopsys' share in this market has already experienced a decrease, from [40-50]% in 2021 to [40-50]% in 2023. At the same time, Empyrean has been significantly increasing its market share, having raised from [0-5]% in 2021 to [10-20]% in 2023.

(314) In the second place, customers regularly evaluate PowerVolt, PTM and Polas alongside Power Device Workbench, and have selected these solutions over PDW. [Synopsys customer engagements].[281]

(315) In the third place, Synopsys monitors and benchmarks Power Device Workbench against Jedat, Primarius/Magwel, and Empyrean's tools. Internal documents show that, [Synopsys competitive assessment].[282]

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278 Form CO, para. 480.

279 Form CO, para. 479.

280 Replies to Questionnaire to customers of EDA and design IP, question D.A.E.1.

281 Parties' Reply to Commission's RFI 26, para. 1.3.

282 Synopsys internal document, Annex RFI 26 Q 1.1; and Synopsys internal document Annex RFI 26 Q 1.2. Also, Parties' Reply to Commission's RFI 26, Figure 1.

(316) In the fourth place, when asked to rate the strength/quality of power device analysis tools, respondents who expressed a view gave higher and similar ratings to Jedat's PowerVolt and Synopsys' Power Device Workbench. Ansys' PowerX and Primarius PTM received similar lower ratings. Empyrean's Polas was rated the lowest.[283]

(317) **Fourth**, the majority of respondents to the market investigation who expressed a view replied that the Transaction would have a "Neutral" impact in the market for power device analysis. Some respondents considered that the Transaction would be "Positive" for this market, namely pointing out that the Merger Entity would prove more comprehensive solutions for power device analysis, potentially streamlining workflows for engineers and, generally, that the Transaction would foster greater innovation.[284]

5.3.2.7.3. Conclusion

(318) In view of the above considerations and in light of the results of the market investigation and the evidence and information available to it, the Commission concludes that the Transaction does not raise serious doubts as to its compatibility with the internal market resulting from horizontal non-coordinated effects on the global market for the supply of power device analysis.

5.3.2.8. Global market for the supply of parasitic analysis tools

(319) Parasitic analysis tools focus on analysing parasitic effects in the design of a chip, i.e., unintended physical properties that can arise in relation to the wiring that connects various components, which can affect a chip's functionality, timing, power consumption, and reliability.[285]

(320) In this market, Synopsys' offers Pillar, a tool that identifies parasitic effects and, allows customers to modify their designs to fix these issues. Ansys' Paragon X identifies parasitics and assists the customer in modifying the chip design (i.e. debugging the effects).[286]

5.3.2.8.1. The Notifying Party's view

(321) The Notifying Party considers that the Transaction will not give rise to any competition concerns in the market for parasitic analysis tools.

(322) **First**, the Transaction only gives rise to a *de minimis* increment due to Pillar's [Synopsys' product-level sales] in 2023. The Transaction will not significantly increase the Parties' market power, nor have any material impact on the existing competitive landscape.[287]

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283 Replies to Questionnaire to customers of EDA and design IP, question D.A.E.2.

284 Replies to Questionnaire to customers of EDA and design IP, question E.3. and E.4.

285 Form CO, para. 452. Parasitic effects include (i) resistances: the loss of power when electricity flows through the wires; (ii) capacitances: unintended cross-talk between different parallel wires; and (iii) inductances: impeding or slowing down the change in electric current flowing through the wire.

286 Form CO, para. 455 and 456.

287 Form CO, para. 459.

(323) **Second**, the Parties do not compete closely. Ansys' ParagonX is able to identify complex parasitic issues very quickly and offers a range of advanced capabilities that Synopsys' Pillar cannot provide (e.g., resistance mapping, detailed visualisation, RC delay analysis, and parasitic impact ranking). In contrast, Pillar does not provide as detailed a range of analyses as ParagonX. Pillar only offers a small number of the features that ParagonX provides.[288]

(324) **Third,** the Merged Entity will continue to face strong competition from other market players, in particular Silvaco and Cadence.

5.3.2.8.2. The Commission's assessment

(325) The Commission considers that the Transaction does not raise serious doubts as to its compatibility with the internal market in the global market for the supply of parasitic analysis tools for the following reasons.

(326) **First**, the Transaction will result in a negligeable increment. As shown in Table 5 above, in 2023, while the Merged Entity will have a combined market share of [70-80]%, the Transaction will result in an increment of merely [0-5]% coming from Synopsys' Pillar tool.

(327) **Second**, the Parties' tools do not appear to compete closely. This is indicated by the very limited share of Synopsys' Pillar as well as the existence of other market players, such as Cadence, Siemens and Silvaco, who would compete more closely with Ansys' ParagonX.

(328) Pillar only offers a small number of the features that Paragon X. Ansys' ParagonX is able to identify complex parasitic issues very quickly and offers a range of advanced capabilities that Synopsys' Pillar cannot provide (e.g., resistance mapping, detailed visualization, RC delay analysis, and parasitic impact ranking). Accordingly, Paragon X allows for use in complex chip designs, namely modern chips for high-performance computing (HPC), AI, automotive, mobile, and Internet-of-Things (IoT). Conversely, Pillar is typically used by customers designing image sensors and analog mixed-signal designs, where parasitics are not a critical component of the design.[289]

(329) **Third**, the Commission considers that post-Transaction there will be enough credible alternatives remaining in the global market of supply of parasitic analysis tools, as Siemens, Cadence and Silvaco are also active in this market and that both Siemens and Cadence's tools are part of integrated offers, as explained below.

(330) Both Cadence and Siemens have a market share of [10-20]% each (Table 5 above). Cadence offers parasitic analysis capabilities, including through its Virtuoso Electrically Aware Design ("EAD") tool and Parasitic Aware Design / SmartView capabilities. These tools have a significant advantage over the Parties' tools, as they are seamlessly integrated with Cadence's popular Virtuoso design platform, which has a leading share and strong competitive position due to its large installed base. Cadence's parasitic analysis features are built into Virtuoso's design cockpit

288 Form CO, para. 460.

289 Form CO, para. 460 and Parties' Reply to Commission's RFI 26, para. 2.11 and 2.12.

and are highly valued by customers for ease-of-use. In contrast, Ansys' solutions must run in a separate GUI.[290]

(331) Siemens Calibre xRC offers parasitic extraction and parasitic analysis in one single tool and can be used in any chip design flow. It is integrated with other Siemens tools, namely graphic user interfaces (Calibre Interactive and Calibre Results Viewing Environment (RVE)) and physical verification tools (Calibre nmLVS). It is certified by all major foundries.[291]

(332) Silvaco's edXact tool has a [0-5]% market share. It offers a broad range of parasitic analysis capabilities (such as resistance mapping, parasitics visualisation, and RC delay analysis), and benefits from high capacity and easy integration into customers' design flows. It is also compatible with a wide range of different parasitic extraction tools, which allow it to be used flexibly by customers.[292]

(333) **Fourth,** market players did not raise any concerns with regards to this market.[293]

5.3.2.8.3. Conclusion

(334) In view of the above considerations and in light of the results of the market investigation and the evidence and information available to it, the Commission concludes that the Transaction does not raise serious doubts as to its compatibility with the internal market resulting from horizontal non-coordinated effects on the global market for the supply of parasitic analysis tools.

5.3.2.9. Global market for the supply of functional safety specification and analysis tools

(335) Functional safety specification and analysis tools are used to ensure chip designs meet different product functional safety standards (e.g., standards set by the ISO and the International Electrotechnical Commission ("IEC")). These tools vary from those which offer broad capabilities to address many functional safety standards for varying purposes, to more specialised EDA tools address individual standards for specific products.

(336) Synopsys' offers VC Functional Safety Manager, which is used to specifically assess relevant functional safety certification for chips. Ansys offers medini analyse, a broad-purpose functional safety analysis tool that allows for consistent and efficient application of industry guidelines and standards in safety critical electronic and software-controlled systems.[294]

5.3.2.9.1. The Notifying Party's view

(337) The Notifying Party considers that the Transaction will not give rise to any competition concerns in the market for functional safety specification and analysis tools.

(338) **First**, the Parties tools have different areas of application, technical capabilities and customers. There is only a very small functional overlap between their capabilities.

290 Form CO, para. 461.
291 Parties' response to the European Commission's RFI 26, para. 2.6 and 2.7.
292 Form CO, para. 461.
293 Replies to Questionnaire to customers of EDA and design IP, question E.4.
294 Form CO, para. 464 and 465.

Due to their significantly different scope and application, the Parties' tools [The Parties' customers' preferences].[295]

(339) **Second**, the Merged Entity will continue to face significant competition from a wide range of competitors in this space including in-house solutions based on Microsoft's Excel and broader-application safety analysis tools (e.g., EnCO Safety Office's SoX, Vector PREEVision Safety Extensions, Isograph' Reliability Workbench) and other specialised tools for chip-related safety analysis (e.g., Cadence's Midas Platform, Siemens' Austemper).[296]

5.3.2.9.2. The Commission's assessment

(340) The Commission considers that the Transaction does not raise serious doubts as to its compatibility with the internal market on the global market for the supply of functional safety specification and analysis tools for the following reasons.

(341) **First**, the Transaction leads to a moderate combined market share in the global market for the supply of functional safety and specification analysis. As shown in Table 9 above, in 2023, the combined market share was [20-30]%. According to paragraph 18 of the Horizontal Merger Guidelines, when the market share does not exceed 25%, the concentration "*may be presumed to be compatible with the common market*".[297]

(342) **Second**, the Commission considers that post-Transaction there will be enough credible alternatives remaining in the global market of supply of functional safety specification and analysis and the Merged Entity will continue to face significant competition from other market players, particularly from Cadence (Midas), with a [40-50]% market share, and Siemens (Austemper), with a [20-30]% market share, in 2023.

(343) **Third,** market players did not raise any concerns with regards to this market.[298]

5.3.2.9.3. Conclusion

(344) In view of the above considerations and in light of the results of the market investigation and the evidence and information available to it, the Commission concludes that the Transaction does not raise serious doubts as to its compatibility with the internal market resulting from horizontal non-coordinated effects on the global market for the supply of functional safety specification and analysis tools.

5.3.3. Potential horizontal overlaps relating to the markets for [functionality] analysis and for [functionality] analysis

5.3.3.1. The Parties' activities

(345) Multiphysics effects involved in multi-die chip designs are closely interrelated due to the proximity of dies and high density of wires connecting those dies, contributing to the fluidity of the segmentations. Accordingly, multi-die

295 Form CO, paras 470 and 471.
296 Form CO. paragraph 472.
297 Horizontal Merger Guidelines, paragraph 18.
298 Replies to Questionnaire to customers of EDA and design IP, question E.4.

functionality markets encompass tools offering several types of analysis.[299] In this Section, and in view of Ansys' activities and Synopsys [business strategy], we will focus on the markets for: (i)[functionality] analysis; and (ii) [functionality], both specific to multi-die chip design:

(a) [functionality] **analysis** assesses how the multi-die chip [functionality of analysis];[300]

(b) [functionality] **analysis** comprises tools that ensure [functionality of analysis]. This covers:[301]

– Electromagnetic analysis, which ensures signal integrity by assessing the effects of resistance, capacitance and inductance, and models and simulates electromagnetic effects that may impact the chip. Multi-die designs are more vulnerable to electromagnetic effects because the current in the wires connecting the dies travels at a very high speed for longer distances, creating strong electromagnetic fields that can disrupt a die's power or signal integrity;

– Power-related effects, namely power consumption profile and power integrity of multi-die chips are critical as the chip's power specifications will impact other characteristics of the chips, such as thermal and electromigration characteristics. As explained in Section 5.3.2.5. above, power integrity analysis checks a chip's reliability when using power, to ensure it will continue to function correctly. This includes checking that the chip will not succumb to electromigration or a drop in voltage (as called "EM/IR").

(346) In these markets, Ansys offers the following products:

- [Ansys products in the markets that raise potential overlaps with Synopsys].[302]
- [Ansys products in the markets that raise potential overlaps with Synopsys].[303]
- [Ansys products in the markets that raise potential overlaps with Synopsys].[304]
- [Ansys products in the markets that raise potential overlaps with Synopsys].[305]
- [Ansys products in the markets that raise potential overlaps with Synopsys].[306]

(347) As presented in Tables 10 and 11 above, Ansys' tools have a [70-80]% market share in the market for [functionality] analysis and a [30-40]% market share in the market for [functionality].

(348) In addition, Ansys has been pursuing a [Ansys' business strategy that raises a potential overlap with Synopsys], which is directed at allowing [Ansys' business

299 Parties' response to the European Commission's RFI 18, para. 5.1.
300 Form CO, para. 72.
301 Parties' response to the European Commission's RFI 18, para. 5.2.
302 Form CO, para. 251 and 627 and Parties' response to the European Commission's RFI 25, para. 15.3.
303 Form CO, para. 1088. Chip design is only one of its use cases, accounting for ~[0-5]% of its revenue in 2023.
304 Form CO, para. 1088. Chip design is only one of its use cases, accounting for ~[10-20]% of its revenue in 2023.
305 Form CO, para. 627.
306 Form CO, para. 627.

strategy]. As part of this strategy, Ansys has been working on [Ansys' business strategy]. In particular, Ansys has been developing [Ansys' business strategy].[307][308]

(349) Synopsys is currently not active in the markets for [functionality] analysis and [functionality]. However, Synopsys was pursuing three R&D Projects [description of Synopsys' business strategy].[309]

5.3.3.2. Legal framework

(350) The Horizontal Merger Guidelines provide that a merger with a potential competitor can generate horizontal anti-competitive effects either: (i) where the potential competitor already significantly constrains the behaviour of the firms active in the market or (ii) where there is a significant likelihood that the potential competitor would enter the market in a relatively short period of time after which the potential competitor would constrain the behaviour of the firm currently active in the market.[310] The Horizontal Merger Guidelines further set out that "*[e]vidence that a potential competitor has plans to enter a market in a significant way could help the Commission to reach such a conclusion*".[311] In either case, there must not be a sufficient number of other potential competitors, which could maintain sufficient competitive pressure after the merger.[312]

(351) According to established case-law of the EU Courts,[313] in cases of potential competition between undertakings which are not active in the same product market,[314] the Commission is required to determine whether, if the absence of the concentration, there would have been real concrete possibilities for it to enter that market and to compete with established undertakings.[315] In other words, there can be no finding of a potential competitive relationship as an inference merely from the purely hypothetical possibility of such entry or even from the mere wish or desire of the undertaking to enter the market. The assessment as to whether there is

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307 Form CO, para. 743.

308 Form CO, para. 740 and 743 and Synopsys' Reply to FTC letter on potential competition, dated 6 Decembre 2024. Ansys has developed optiSLang, which is a design optimisation product that leverages AI techniques to perform design space optimisation – that is identify the optimal design configurations for a user identified target. It can be deployed in a variety of applications and there are optiSLang workflows for several Ansys tools. There are currently workflows with RedHawk(-SC) and RedHawk-SC Electrothermal.

309 Form CO, para. 657.

310 Horizontal Merger Guidelines, paragraph 59 and 60.

311 Horizontal Merger Guidelines, paragraph 60.

312 Horizontal Merger Guidelines, paragraph 60.

313 See, e.g., General Court judgments of 15 September 1998, *European Night Services and Others* v *Commission* (T-374/94, T-375/94, T-384/94 and T-388/94, EU:T:1998:198), paragraphs 137 to 142; of 22 March 2011, *Altstoff Recycling Austria* v *Commission* (T-419/03, EU:T:2011:102), paragraph 65; of 14 April 2011, *Visa Europe and Visa International Service* v *Commission* (T-461/07, EU:T:2011:181), paragraphs 22 and 83; of 29 June 2012, *E.ON Ruhrgas and E.ON* v *Commission* (T-360/09, EU:T:2012:332), paragraphs 86 and 87; of 28 June 2016, *Portugal Telecom* v *Commission* (T-208/13, EU:T:2016:368, paragraphs 181 and 186; and Court of Justice judgment of 30 January 2020, *Generics (UK) e.a.* v *CMA* (C-307/18, ECLI:EU:C:2020:52) paragraphs 35 to 39; and General Court judgment of 13 November 2024, Deutsche Telekom AG v CMA (T-64/20, ECLI:EU:T:2024:815), paragraphs 135 to 142.

314 Potential competition can also exist between undertakings active in the same product market albeit in different geographic markets, in which case the question of potential market entry becomes one of potential geographic expansion.

315 General Court judgment of 13 November 2024, *Deutsche Telekom AG* v *CMA* (T-64/20, ECLI:EU:T:2024:815), paragraph 135 and Court of Justice judgment of 30 January 2020, *Generics (UK) e.a.* v *CMA* (C-307/18, ECLI:EU:C:2020:52) paragraph 36

potential competition must be supported by factual evidence or an analysis of the structure of the relevant market and the economic and legal context within which the undertakings operate.[316]

(352) Depending on the circumstances of the case, the Commission may rely on a number of elements to establish whether there is potential competition between two undertakings,[317] such as whether or not entry into a market is an economically viable strategy,[318]the undertaking's intentions, the existence of preparatory steps already undertaken to enter the market in a sufficiently short period of time in the light of the characteristics of the market, or even the perception of undertakings (namely competitors) already present in the market.[319]

5.3.3.3. The Notifying Party's view

(353) The Notifying Party submits that the Trans-action will not result in the loss of future competition between the Parties, as Synopsys does not compete with Ansys in S&A tools (which is Ansys' main focus of activity) and is not a credible future entrant in EDA the markets for [functionality] analysis and [functionality]. Likewise, Ansys also does not have plans to compete with Synopsys in any addition EDA markets.[320]

(354) **First**, Synopsys' R&D projects are intended to complement, and not compete with, Ansys sign-off tools which offer [functionality] analysis and [functionality] for chip design. Projects [project names] relate to the development of [nature of tool]. By contrast, tools providing [functionality] analysis and/or [functionality] for chip design – such as those offered by Ansys, Cadence and Siemens – are [nature of tool] tools designed to deliver highly accurate and detailed analysis of physical effects. These tools are typically used at the physical verification and sign-off stage of the chip design flow, to ensure that the (near)completed chip design complies with foundry requirements and, conversely, are not [purpose of R&D projects demonstrating the absence of competition concerns from any potential overlap with Ansys].[321]

(355) **Second**, Synopsys relies on its partnership with Ansys for [functionality] for the design of multi-die chips. Under this partnership, Synopsys and Ansys developed a number of supported work-flows between 3DIC Compiler and Ansys' sign-off tools, namely RedHawk(-SC), RedHawk-SC Electrothermal, and HFSS, to enable a

316 General Court judgment of 29 June 2012, *E.ON Ruhrgas and E.ON v Commission* (T-360/09, EU:T:2012:332), paragraph 86; Court of Justice judgment of 30 January 2020, *Generics (UK) e.a.* v *CMA* (C-307/18, ECLI:EU:C:2020:52) paragraphs 38 and 39 and General Court judgment of 13 November 2024, Deutsche Telekom AG v CMA (T-64/20, ECLI:EU:T:2024:815), paragraph 135.

317 See, to that effect, Court of Justice judgments *EDP - Energias de Portugal and Others* (C-331/21, ECLI:EU:C:2023:812), paragraphs 63 and 65, and of 27 June 2024, *Servier and Others* v *Commission* (C-201/19 P, ECLI:EU:C:2024:552), paragraph 124.

318 General Court judgments of 29 June 2012, *E.ON Ruhrgas and E.ON v Commission* (T-360/09, EU:T:2012:332), paragraph 86 and of 13 November 2024, Deutsche Telekom AG v CMA (T-64/20, ECLI:EU:T:2024:815), paragraph 136.

319 Court of Justice judgment *EDP - Energias de Portugal and Others* (C-331/21, ECLI:EU:C:2023:812), paragraphs 69 et seq.

320 Form CO, para. 653.

321 Form CO, para. 715 and 716.

more seam-less use of Ansys' multiphysics analysis capabilities with Synopsys' implementation solution for multi-die chips.[322]

(356) **Third**, the Notifying Party submits that these R&D projects are nascent and have significant lead-times. It would take a long time for Synopsys to develop solutions that could compete with rivals such as Cadence and Siemens, [description of Synopsys business strategy].[323]

(357) **Fourth**, Synopsys has no plans to [description of Synopsys business strategy demonstrating the absence of competition concerns from any potential overlap with Ansys.[324]

(358) **Fifth**, [description of Synopsys commercial assessment and Ansys business strategy demonstrating that Ansys is not a potential competitor of Synopsys in EDA]. Ansys' semiconductor offering is focused on multiphysics S&A tools used at the sign-off stage. [Description of Ansys commercial plans demonstrating that Ansys is not a potential competitor of Synopsys in EDA].[325]

5.3.3.4. The Commission's assessment

(359) For the reasons explained below, the Commission considers that the Transaction does not raise serious doubts as to its compatibility with the internal market due to the elimination of Synopsys as a potential competitor in the markets for [functionality] analysis and [functionality] analysis tools for multi-die chip design, given that the R&D projects being pursued by Synopsys are directed at [Synopsys' business strategy], which are not active in the aforementioned markets.

(360) The Commission also considers that [Ansys' business strategy] would not entail an entry into any new market, given that [details of Ansys business' strategy].

5.3.3.4.1. Context

(361) As a general context, the Commission notes that multi-die chip design has been identified by the Parties and other market participants (both customers and competitors) as one of the main market trends in semiconductors and chip design, which is expected to play a crucial role in driving the growth of the EDA market. Synopsys expects that by 2029, EDA tools used for multi-die chips will account for ~[30-40]% of sales of all EDA tools, and that the CAGR for EDA tools for multi-die will be + [40-50]% over the period 2023-2029; compared to + [5-10]% for the remaining EDA tools.[326]

(362) While multi-die designs offer several advantages, in terms of higher performance and lower costs over time, these also pose additional challenges due to their complex architecture.[327] Accordingly, these designs require more frequent and intensive multiphysics analysis, which typically include thermal analysis, signal and power integrity analysis and electromagnetic analysis. The type of

322 Form CO, para. 546.
323 Form CO, para. 718 and Synopsys submission to the CMA on potential future competition, submitted 8 November 2024 ("**Submission on Potential Competition**"), para. 2.6.
324 Form CO, para. 720.
325 Form CO, para. 723 and 736.
326 Form CO, Annexes M.11481 - 4(c)-10 […], slide 18.
327 Form CO, para. 52 and 55.

multiphysics analysis that customers seek varies throughout the design process. In the earlier stages of the design process, customers seek fast ("coarse") analysis capabilities to get directional information about the multiphysics characteristics of alternative designs, and flag potential problems. As customers start implementing the design, they need more accurate (but necessarily slower) multiphysics data. At the very end of the design process, before tape-out, customers need highly accurate sign-off tools (which are certified by foundries) to validate the design.[328]

(363) Cadence and Siemens have been heavily investing in multiphysics capabilities and currently have integrated offers for multi-die chip design, namely Integrity 3D-IC and Innovator 3D-IC respectively, offering tools for thermal analysis and electromagnetic analysis (which are also part of those integrated offers) [329] Integrity 3D-IC offers both early-stage analysis during the design stage (i.e., as natively embedded capabilities in Integrity 3D-IC), and full-chip analysis at the sign-off stage through using its standalone thermal (Celsius), power/IR drop (Voltus), electromagnetic (Clarity) and signal integrity (Sigrity) S&A sign-off tools.[330]

(364) Siemens launched its tool Innovator3D IC in June 2024. Siemens claims it offers a "*comprehensive multiphysics cockpit*" with early-stage analysis through "*unifying power, signal, thermal, and mechanical stress analysis tools, [enabling] rapid 'what-if' exploration, while identifying, avoiding and solving challenges prior to detailed design implementation*."[331] Innovator3D IC combines capabilities from Siemens Aprisa place-and-route tool, Xpedition package design software, Calibre physical verification tool, NX mechanical design tool, and Tessent test software.[332]

(365) As submitted by the Notifying Party, part of the Transaction rationale is to allow Synopsys to better address the growth in multi-die chips, which require increased multiphysics analysis capabilities, which can be offered by Ansys. [333] Post-Transaction, to address multiphysics challenges relating to multi-die chip designs, Synopsys is planning to [Synopsys' product development plans].[334].[335]

(366) The Notifying Party submits it evaluated other options to develop [Synopsys' business strategy]. In addition to the acquisition of Ansys, Synopsys considered the option [Synopsys' business strategy]. The Notifying Party submits that both other options would have been "*insufficient to meet customer requirements and competitive benchmarks*".[336]

(367) In light of the legal framework laid out above, the Commission will analyse [Synopsys' business strategy], in order to assess the existence of "real and concrete" possibilities of Synopsys entering the markets for [functionality] analysis and/or [functionality] for multi-die chip design.

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328 Form CO, para. 57.
329 Form CO, para. 631.
330 Submission on Potential Competition, para. 2.7.
331 Siemens' website, available at (last access 12.12.2024): https://newsroom.sw.siemens.com/en-US/innovator3d-ic/.
332 Submission on potential competition, para. 2.8.
333 Form CO, para. 49.
334 Form CO, para. 560.
335 Form CO, para. 548.
336 Form CO, para. 555.

(368) In addition, the Commission shall assess whether [Ansys' business strategy] would lead Ansys to start offering tools in any new EDA markets for multi-die chip design, where they could become an effective competitor of Synopsys.

5.3.3.4.2. Unlikelihood of Synopsys to grow into an effective competitor of Ansys in [functionality] analysis and [functionality], absent the Transaction

5.3.3.4.2.1. [Project name] – potential entry in the market for [functionalities] analysis

(369) The Notifying Party describes Project [project name] as intended to [purpose of R&D project demonstrating the absence of competition concerns from any potential overlap with Ansys] particularly targeted for multi-die designs.[337]

(370) The initial idea for the project was presented internally in [description of Synopsys project development process and project status].[338] [339].[340]

(371) The Notifying Party submits that Project [project name] would not be available [description of how product developed will be offered] but would rather be [description of internal project], in relation to which Ansys does not offer any competing products. [Description of functionality provided by internal project] The Notifying Party submits that Ansys does not offer any competing products to [internal project].[341]

(372) Ansys is present in the market for [functionality] analysis for multi-die chip design with its [names of Ansys tools].

(373) In this context, and in line with the case-law cited above, the Commission will assess the existence of potential competition in view of the circumstances of the present case

(374) **First**, the Commission considers that while there are internal documents of Synopsys which may indicate that Project [project name] could be further developed into [product/functionality that could potentially compete with Ansys' tools] these do not translate into sufficiently concrete plans to develop a [product/functionality] that would enter the market for [functionality] and compete with Ansys' sign-off tools for multi-die chip design.

(375) <u>In the first place,</u> Synopsys' internal documents related to Project [project name] generally confirm that the aim of this project is to provide [Synopsys' business strategy demonstrating the absence of potential competition concerns with Ansys' tools]. For instance:

(a) An internal presentation titled [document title] dated of November 2023, shows the target of [description of objectives of internal project]. This presentation also includes a [description of plans for internal project].[342]

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337 Form CO, para. 666

338 Form CO, Table 36.

339 The Notifying Party submits that, in contrast to foundry certification, enablement is a less rigorous process of confirming the general accuracy of tools/capabilities and enabling them for us in customer design flows.

340 Form CO, Table 36.

341 Form CO, para. 666

342 Synopsys internal document, "[…]", dated of November 2023, slides 4 and 44.

(b) In a Synopsys internal email from [names and titles of Synopsys senior management], dated 21 November 2023, in which [Synopsys manager] asks for confirmation on the timeline target of each of the three R&D projects, Project [project name]'s goal is stated as to [description of project objective]. The timeline target to be confirmed is [time period].[343]

(c) An internal presentation titled [document title], dated 6 September 2023, explains [description of objectives of internal project] by identifying the problem Project [project name] is trying to solve [description of objectives of internal project]. This document clearly show that Project [project name] relates to [capabilities], as it identifies as the solution for the aforementioned problem [description of objectives of internal project] specifically in [tools name].[344]

(d) An internal presentation titled [document title], dated June 2023, presents Synopsys [description of project objectives] and explains that [description of project objectives]. The presentation clearly shows [capabilities] as part of the analysis to [description of project objectives].[345]

(e) An internal presentation titled [document title], dated 14 November 2022, shows [description of internal project plans];[346]

(f) An internal presentation titled [document's title], dated 28 June 2021, shows the plans for Project [project name] to [description of internal project plans].[347]

(376) The [capabilities] mentioned in Project [project name] in Synopsys' internal documents described above refer to [Synopsys' business strategy] as follows:

(a) [A first capability] relates to Project [project name and description of internal project capabilities] which would allow designers to receive input on [description of internal project objectives] which is particularly important due to the complexity of multi-die design and the need for [description of internal project objectives*]*;

(b) [A second capability] relates to Project [project name and description of internal project capabilities] which will allow designers to receive input on [description of internal project objectives];

(c) [A third capability] relates to Project [project name and description of internal project capabilities] which will [description of internal project objectives.[348]

(377) In the second place, some internal documents show the complementarity between Project [project name and capabilities] and Ansys' sign off tools. For instance, an internal presentation titled [document title], dated November 2023 (Figure 8 below) shows Project [project name] (as well as Project [project name] [description of internal projects capabilities], which will be together with Ansys' tools, for sign-off stage. This figure appears in other Synopsys' internal documents, including in

343 Synopsys internal document, SNPSCMA-00012334, […], dated 21 November 2023.
344 Synopsys internal document, Annex PN RFI 4 - Q.16-002, […], 6 September 2023", slide 7 to 10.
345 Synopsys internal document, SNPSCMA-00011784, titled […], dated June 2023, slide 14.
346 Synopsys internal document, Annex PN RFI 4 - Q.16-001, […], 14 November 2022, slide 4.
347 Synopsys internal document, SNPSCMA-00003614, […], 28 June 2021, slide 10.
348 Synopsys' Letter to the FTC on […], dated 18 November 2024, submitted to the EC on 19 November 2024.

presentation to [Synopsys' customers], which are significant customers of Synopsys.[349]

Figure 8: [Complementarity between Synopsys' business strategy and Ansys tools]

[…]

Source: Synopsys internal document, SNPSCMA-00010029, titled […]*, dated November 2023, slide 14 (ID 1510-320)*

(378) In the third place, only very limited internal documents of Synopsys include references to the possibility of Project [project name] as a [description of product that could potentially compete with Ansys' tools] and, even in this case, such documents appear to relate to the possibility of a [description of potentially competing product functionality] which has not moved forward. Specifically:

(a) In a presentation for [Synopsys' management], titled [document title], dated of October 2023, where Synopsys presents its [capabilities], it is stated [description of Synopsys' internal document confirming Synopsys' business strategy]. [350] .[351]

(b) In a presentation on Project [project name], dated November 2022, which presents [description of internal project] it is clearly stated that [description of Synopsys' internal project] showing that the purpose of Project [project name], was [Synopsys business strategy][352].

(c) In presentation a titled [document title], dated 15 March 2022, one slide is titled [title of the presentation]. However, there was no timeline associated with [Synopsys business strategy] and some tasks are still "TBD". The Notifying Party further clarified that this document is referring to [project name]'s ability to [description of functionalities demonstrating the absence of potential competition concerns with Ansys tools]. [353].[354]

(379) In the fourth place, internal documents from Synopsys' relating to discussions with foundries [description of foundry engagement with project] do not address [description of product functionality that could potentially compete with Ansys tools] but rather [other capabilities]. Specifically:

(a) In an email dated 22 April 2024 from [customer's employee name] to [Synopsys' employee name] (Synopsys), it is stated that [description of internal project capabilities]. This email was forwarded in 23 April 2024, by [Synopsys' employee name] to [another Synopsys' employee name] with the statement that [description of the internal project]. As submitted by the Notifying Party, this document does not refer to [project final status], as clarified later in the same e-mail chain, the results reported in [customer's employee] email refer only to [project name] having [description of the internal project capabilities], which refer to [project name]'s [capabilities]

349 [Synopsys internal documents].
350 Synopsys internal document, M.11481 - […], of October 23, slide 31.
351 Response to CMA Issues Letter, para. 8.12.
352 Synopsys internal document, Annex PN RFI 4 - Q.16-001, […], 14 November 2022, slide 18.
353 Synopsys internal document, SNPSCMA-00006295, […], March 2022, slide 6.
354 Parties' response to the European Commission's RFI 25, para. 13.2.

that [description of preliminary project status]. This refers to [description of status and processes].[355].[356]

(b) An internal presentation titled [document title], dated of November 2023, shows that generic reference to [capabilities] refers to the [description of project capabilities that do not compete with Ansys].[357]

(c) An internal presentation titled [document title], of 6 September 2023, by [Synopsys' employee name and title], includes a slide on [presentation title], discussing status of [foundry engagement]. The presentation clearly shows that Project [project name] is intended to be a [description of project objectives]. Therefore, the status of [description of foundry engagement] relate to these [capabilities], rather than [functionalities that could be competing with Ansys];[358]

(d) An internal presentation titled [document title], of March 2022, includes a slide on [presentation title], which explains that [description of foundry engagement]. In another slide, it can be seen that they key features developments regarding such [foundry engagement] relate to [capabilities that do not compete with Ansys];[359]

(e) In another presentation, titled [document title] of March 2022, presents the [internal project results], showcases Project [project name] [capabilities];[360]

(380) In the fifth place, the Commission considers that [description of product/functionality that would potentially compete with Ansys' tools], which were being developed under Project [project name], do not substitute [Ansys tool capabilities] which is needed to meet foundry requirements for manufacture.

(381) This is made clear by Synopsys' internal documents showing complementarity between [the capabilities of the internal project under development] and the current design flows enabled by the partnership with Ansys, under which [Ansys' tool] is used for [functionality].[361]

(382) In view of the above, the Commission considers that the [functionality] developed under Project [project name] were merely intended to [description of project objectives demonstrating absence of potential competition with Ansys]. Accordingly, such capabilities would be [description of project objectives] which are not active, nor would be active, in the market for [functionality] analysis, as these would not provide [functionality] sign-off and compete with Ansys' [tool], Cadence's [tool] and Siemens' [tool], which are the main players in the market.

(383) These capabilities will rather allow [description of project objectives], particularly [name of Synopsys tools], to compete more closely with competing tools for [functionalities], i.e., respectively, with Cadence's [tools] and Siemens [tools].

(384) **Second**, the Commission considers that Synopsys would not have the incentives to build a [description of internal project] tool for [functionality] analysis in multi-die

355 Synopsys internal document, SNPS-FTC-34675457.
356 Parties' response to the European Commission's RFI 25, para. 8.1.
357 Synopsys internal document, […], dated of November 2023, slides 45 and 48.
358 Synopsys internal document, Annex PN RFI 4 - Q.16-002, […] 6 September 2023, slide 22/
359 Synopsys internal document, SNPSCMA-00006205, […] of March 22, slides 6 and 9.
360 Synopsys internal document, Annex PN RFI 4 - Q.16-003, […] of March 2022, slides 2 and 9.
361 [Synopsys internal documents].

chip design, which means that economic viability of entry in this market would be merely hypothetical.

(385) In the first place, the Commission notes that Synop-ys' partnership with Ansys provides Synopsys customers with access to Ansys' multiphysics sign-off tools such as RedHawk(-SC), RedHawk-SC Electrothermal and HFSS. Under the partnering with Ansys, in which Synopsys [Synopsys' business strategy], it is able to meet customers' needs for these sign-off capabilities which it is not able to provide itself.

(386) In fact, internal documents assessing counterfactual scenarios show that, absent the Transaction, Synopsys did not contemplate the development of a [functionality] analysis tool which would allow Synopsys to enter the market for [functionality] analysis and compete with Ansys' standalone tools for multi-die. These documents evidence that Synopsys intended to [description of project objectives], to meet customer requirements and better compete with Cadence and Siemens. For this, Synopsys contemplated three scenarios: [Synopsys' business strategy]. Therefore, none of the counterfactual scenarios to the Transaction were the development of [tools competing with Ansys].[362]

(387) In the second place, even though multi-die chip design is a main new market trend in which Synopsys has been heavily investing and innovating in this field, there is no evidence that Synopsys would have a strategic interest to enter the market for [functionality] analysis for multi-die chip design or that such entry would be economically viable.[363]

(388) *Firstly*, apart from the very limited internal documents with references to Project [internal project objectives] – which have been analysed above – no internal documents evidence a strategic interest of Synopsys in developing a [feature] sign-off tool for [functionality] analysis.

(389) Testimonials of Synopsys' executives before the FTC indicated that Synopsys' management never considered Project [project name] as an attempt to build a [functionality] sign-off tool; never considered expanding the scope to include the development of a [functionality] sign-off tool; and indicated its R&D efforts on developing a [internal project].[364]

(390) *Secondly*, while it has been acknowledged that it would be, in theory, possible to further develop Project [project name] into a sign-off tool, this would require expertise, investment and time. Synopsys' lead engineers [names and titles of Synopsys' engineers] have testified that it would take close to [years] years to develop Project [project name] into a sign-off tool.[365]

(391) This has also been corroborated by market participants. For instance, a market participant explained that while "*Synopsys could start developing its own multi-physics analysis tools for multi-die chip design* […] [f]*or a standalone Synopsys to gain significant market share, it would likely take a decade or more*.".

362 Synopsys internal document, M.11481 - […] of October 23, slide 30, 31 and 32.
363 Form CO, para. 539 to 547.
364 Synopsys' Letter to the FTC on […], submitted to the EC on 19 November 2024.
365 Transcript of […] deposition before the FTC, 25 October 2024 page 114 -115 and transcript of […] deposition before the FTC, 30 October 2024, page 61-62.

(392) *Thirdly*, in the event Synopsys would enter the market for [functionality] analysis for multi-die chip design, it is unclear whether it would be successful and become an effective competitor. While Synopsys has some successful sign-off tools in its portfolio (such as PrimeTime or PrimePower) it previously had a [functionality] analysis tool, which was moved to end-of-life stage after it failed to gain traction in the market. As previously explained, Synopsys discontinued the tool in favour of the partnership with Ansys, under which it started offering [Ansys' tool] and developed [Ansys' tool].[366]

(393) In view of the above, the Commission considers that would not have 'real and concrete possibilities' to enter the market for [functionality] analysis for multi-die chip design and to compete with established undertakings in that market.

5.3.3.4.2.2. Project [project name] – potential entry in the markets for [functionality] analysis

(394) The Notifying Party describes Project [project name] as intended to provide [description of internal project].[367]

(395) Synopsys acquired part of part of [Synopsys business strategy for internal project development]. These assets that Synopsys acquired concern [acquired assets] for [internal project development] used to analyze [functionality] in multi-die chips.[368]

(396) [One of assets acquired] provides on-chip [functionality] analysis for [application of functionality]. The tool is therefore used in the design of [description of application of functionality]. The Parties acknowledge that [the product] provides similar functionality to Ansys' [tool name].[369]

(397) [One of the assets acquired] provides [functionality] analysis in [application of functionality]. [Description of functionality application]. The Notifying Party claims [the asset] does not provide similar functionality to any Ansys tool.

(398) As part of the deal with [the seller], and as a condition set by [the seller] for Synopsys to obtain the [assets] for the development of Project [project name], [description of agreed terms and conditions for the acquisition of the assets]. The Notifying Party submits that [the assets acquired] have […] revenues, in the entire Fiscal Year 2024, Synopsys generated just […] of revenue from the sale of [acquired assets] to a total of [number] customers. [Description of Synopsys commercial practice under agreed terms and conditions for the asset acquisition].[370]

(399) Project [project name] is at an earlier stage of development than Project [project name]. The initial idea for the Project was presented internally in [information about project development]. The Notifying Party submits that, based on the project team's best estimate, the earliest possible time for Project [project name] to enter the [development stage] (the project's next development stage) is [time period].

366 Synopsys' Letter to the FTC on […], submitted to the EC on 19 November 2024.
367 Form CO, para. 676 and Parties' response to the European Commission's RFI 25, para. 8.18.
368 Form CO, para. 679.
369 Form CO, para. 681.
370 Form CO, para. 684 and Parties' response to the European Commission's RFI 25, para. 15.1.

The Notifying Party submits that it has been liaising with [information about internal project development].[371].[372]

(400) The Notifying submits that it does not intend to offer the capabilities being developed by Project [project name] as [Synopsys' business strategy]. Synopsys intends to [Synopsys' business strategy].[373]

(401) As described above, Ansys offers [functionality] analysis tools, namely [names of Ansys tools and description of their functionalities].

(402) In this context, and in line with the case-law cited above, the Commission will assess the existence of potential competition in view of the circumstances of the present case.

(403) **First**, the Commission considers that **Synopsys did not have concrete plans to further develop Project** [project name] into a standalone and/or sign-off tool which would enter the market for or [functionality] analysis and compete with Ansys' sign-off tools in these markets.

(404) In the first place, Synopsys' internal documents related to Project [project name] confirm that the aim of this project is to provide [description of internal project capabilities], rather than a standalone/sign-off product. For instance:

(a) An internal presentation titled [document title], confirms that the [project name] plan is to [scope of the internal project].[374]

(b) In a Synopsys internal email from [names and titles of Synopsys senior management] dated 21 November 2023, in which [Synopsys manager] asks for confirmation on the timeline target of each of the three R&D projects, Project [project name]'s goal is stated as to [description of project objective]. The timeline target to be confirmed is [time period].[375]

(c) An internal presentation titled [document title], dated of November 2023, shows [scope of the internal project], which is projected for [time period].[376]

(d) An internal email from Synopsys, dated 19 October 2023, circulating the distribution agreement with [seller], explains that [scope of the internal project].[377]

(e) An internal presentation titled [document title], dated June 2023, presents [scope of the internal project].[378]

(405) In the second place, some internal documents clearly show the complementarity between Project [project name and capabilities] and Ansys' sign off tools. For instance, an internal presentation titled [document title], dated November 2023 (Figure 8 below) shows that [project functionality] (under development by Project [project name]) as [description of internal projects capabilities], which will be together with Ansys' tools, for sign-off stage, namely [name of Ansys' tool]. This

371 Form CO, Table 38.
372 Form CO, para. 694.
373 Form CO, para. 675.
374 Synopsys internal document, Annex PN RFI 4 – Q.16-006, […], slide 24.
375 Synopsys internal document, SNPSCMA-00012334, […].
376 Synopsys internal document, […], dated of November 2023, slides 4 and 44.
377 Synopsys internal document, Annex PN RFI 4 – Q.18, […], dated 19 October 2023.
378 Synopsys internal document, SNPSCMA-00011784, titled […], dated June 2023, slide 5, 7 and 9.

figure appears in other Synopsys' internal documents, including in presentation to [Synopsys' customers], which are significant customers of Synopsys.[379]

(406) In the third place, while there are some internal documents of Synopsys comparing or benchmarking [the acquired assets] with those of Ansys, competition between these [assets] and Ansys' tools, namely [Ansys' tool names], has not been confirmed.[380]

(407) *Firstly*, the results of the market investigation show that these tools do not compete with any Ansys' tools for multi-die chip design. When asked about alternatives for Ansys' multi-die chip design tools, no respondent indicated [the acquired assets] would be alternatives to Ansys' [Ansys' tool name].[381]

(408) *Secondly*, the internal documents benchmarking or comparing capabilities of [the acquired assets] with Ansys' [Ansys' tools names] are Synopsys' documents prepared in the context of the transaction with [seller]. As submitted by the Notifying Party, such documents assessed [the acquired assets] based on their suitability to serve as [description of objective for internal project], which would have to communicate with Ansys' tools performing such analysis with focus on accurate final sign-off, in which Synopsys' relied via partnership.[382] [383]

(409) *Thirdly,* Ansys internal documents show that Ansys does not consider [the acquired assets] as a competitor to its tools [Ansys' tool names]. Specifically, these documents only present [names of Ansys' competitors] as competitors to Ansys' [Ansys' tool names].[384]

(410) *Fourthly,* Synopsys' acquisition of [description of commercial terms agreed with seller] is not part of any plans to compete with Ansys' tools. As confirmed by Synopsys internal documents, the [commercial terms] were a condition set by [the seller] for Synopsys to obtain the [assets] on which the development of Project [project name] could be based – which was Synopsys' objective in entering into the transaction with [seller].[385]

(411) In addition, even if we were to consider that [the acquired assets] do compete with Ansys tools, [the commercial terms agreed with the seller] would only give rise to a negligible overlap, given that, as mentioned above, Synopsys only generated USD […] of revenue from the sale of [seller's] products to a total of [number of customers] customers and does not expect it would generate much higher revenue until the expiry of the resell agreement in [expiration year].[386] This is confirmed by the Synopsys internal documents.[387]

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379 [Synopsys internal documents].

380 [Synopsys internal documents].

381 Replies to Questionnaire to customers and competitors of EDA and design IP, question D.A.F.2.

382 Parties' response to the European Commission's RFI 25, para. 15.7.

383 Form CO, para. 546. Specifically, the Parties' partnership allows design data from 3DIC Compiler to be imported into HFSS.

384 [Ansys internal documents].

385 Parties' response to the European Commission's RFI 25, para. 16.1 and 16.3; Synopsys internal document, Annex PN RFI 4 – Q.18 […] email dated 19 October 2023.".

386 Form CO, para. 684 and Parties' response to the European Commission's RFI 26, para. 4.2.

387 Synopsys internal document, Annex PN RFI 4 – Q.18, […] email dated 19 October 2023.

(412) Accordingly, Synopsys is developing these capabilities to improve existing products in different markets rather than the [functionality] market, enabling them to guide design decisions and help design iterations. [Project name] capabilities will [description of internal project]. These tools do not compete with Ansys' [functionality] sign-off solutions [Ansys' tools name].

(413) **Second**, the Commission considers that **Synopsys would not have the incentives** to build a standalone tool for [functionality] analysis, namely to enter the market for [functionality] for multi-die chips, which means that **economic viability of entry in this market would be merely hypothetical**, for the following reasons.

(414) In the first place, Synopsys' already relies in its partnership with Ansys to provides its customers with access to Ansys' multiphysics sign-off tools such as RedHawk(-SC), RedHawk-SC Electrothermal and HFSS. Under the partnership with Ansys, in which Synopsys [Synopsys' business strategy], it is able to meet customers' needs for these sign-off capabilities which it is not able to provide itself.

(415) This is evidenced by internal documents assessing counterfactual scenarios show that, absent the Transaction, Synopsys did not contemplate the development of a [functionality] analysis tool which would allow Synopsys to enter the market for [functionality] analysis and compete with Ansys' standalone sign-off tools for multi-die.

(416) In the second place, even though multi-die chip design is a main new market trend in which Synopsys has been heavily investing and innovating in this field,[388] there is no evidence that Synopsys would have a strategic interest to enter the market for [functionality] analysis for multi-die chip design with a [description of project objectives] capabilities, or that such entry would be economically viable.

(417) *Firstly*, no internal documents evidence a strategic interest of Synopsys in developing a standalone [functionality] analysis tool, which would compete with Ansys' [Ansys' tools name].

(418) *Secondly*, while it may be, in theory, possible to further develop Project *[project name]* into a sign-off tool, this would require significant expertise, investment and time, as submitted by the Parties and corroborated by the feedback of market participants. For instance, a market participant explained that while "*Synopsys could start developing its own multi-physics analysis tools for multi-die chip design* […] [f]*or a standalone Synopsys to gain significant market share, it would likely take a decade or more.*".[389]

(419) In this context, the Commission recalls that while Project [project name] is at a more advanced stage, having functionalities already in [development stages], Project [project name] is at an earlier stage.

(420) *Thirdly*, in the event Synopsys would enter the market for [functionality] analysis for multi-die chip design, it is unclear whether it would be successful and become an effective competitor.

388 Form CO, para. 539 to 547.

389 Market participant's response to the European Commission's RFI 2, para. 23.2.

(421) Accordingly, the Commission considers that the internal documents of Synopsys do not show concrete plans to further develop [project name] that would enter the market for [functionality] analysis in multi-die chip design and become an effective competitor in that market.

(422) The Commission therefore concludes that Synopsys would not have 'real and concrete possibilities' to enter the markets for [functionality] analysis for multi-die chip design and to compete with established undertakings in those markets.

5.3.3.4.2.3. Project [project name] – potential entry in the market for [functionality]

(423) The Notifying Party describes Project [project name] as directed at the development of [description of internal project and functionality that could potentially compete with Ansys].[390]

(424) The Notifying Party submits that it does not intend to offer the capabilities being developed by Project [project name] as a standalone/sign-off product. Synopsys is planning to [description of project objectives demonstrating absence of potential competition with Ansys].[391]

(425) Project [project name] is in the earliest stage of development in comparison to the other two projects. The initial idea for the project was presented internally in [description of Synopsys project development process and project status].[392]

(426) The Notifying Party submits that it has not been in discussion with foundries about "enabling" [project name] as the project is premature for meaningful foundry assessment. Given the very early stage of the project, there is currently no release schedule or product roadmap available.[393]

(427) In this context, and in line with the case-law cited above, the Commission will assess the existence of potential competition in view of the circumstances of the present case.

(428) **First**, the Commission considers that **Synopsys did not have concrete plans to further develop Project** [project name] into a standalone/ sign-off tool which would enter the market for [functionality] analysis and compete with Ansys' sign-off tools for multi-die chip design.

(429) In the first place, Synopsys' internal documents related to Project [project name] generally confirm that the aim of this project is to provide [description of project objectives demonstrating absence of potential competition with Ansys]. For instance:

(a) An internal slide deck of Synopsys, dated 2024, provides an update on the development of [description of internal project].[394]

(b) In a Synopsys internal email from [names and titles of Synopsys senior management] dated 21 November 2023, in which [description of internal project timeline target].[395]

390 Form CO, para. 671.
391 Form CO, para. 672.
392 Form CO, para. 673 and Table 37.
393 Form CO, para. 673.
394 Synopsys internal document, Annex PN RFI 4 - Q.16-014, […] dated 2024, slide 1.

(c) An internal presentation titled [document title], dated of November 2023, lists [description of internal project].[396]

(d) An internal presentation titled [document title], dated 16 November 2023, shows Synopsys plans for the development of [description of internal project].[397]

(e) An internal presentation titled [document title] dated June 2023, presents Synopsys [description of internal project].[398]

(f) In an email dated 23 January 2023, from Synopsys' [names and titles of Synopsys senior management] regarding [description of internal project].”[399]

(430) The internal documents analysed above also show that while there are already roadmaps for Project [project name], these are moving targets and projections for the timeline of development. For instance, the most recent document indicates that [description of internal project]. Such targets have not been met, as the code for Project [project name] is still being developed, as explained above. [400].

(431) In the second place, some internal documents show the complementarity between Project [project name and capabilities] and Ansys' sign off tools. For instance, an internal presentation titled [document title], dated November 2023 (Figure 8 below) shows Project [project name] (as well as Project [project name] [description of internal projects capabilities], which will be together with Ansys' tools, for sign-off stage. This figure appears in other Synopsys' internal documents, including in presentation to [Synopsys' customers], which are significant customers of Synopsys.[401]

(432) In the third place, only one internal document, a presentation for the Board of Directors, titled [document title] dated October 2023, refers to the possibility of Project [project name] as [internal project objectives]. Even in this case, the Notifying Party clarified that this [clarifications provided by Synopsys demonstrating absence of potential competition with Ansys].[402][403]

(433) In the fourth place, internal documents confirm that there were discussions with [Synopsys' customers] as partner customers for preliminary feedback on the capabilities to develop to but there Synopsys had not yet engaged in enablement or “certification” discussions with foundries, due to the early stage in which Project [project name] is in.[404]

(434) In view of the above, the Commission considers that the [functionality] capabilities developed under Project [project name] were merely intended to [description of project objectives demonstrating absence of potential competition with Ansys]. Accordingly, such capabilities would be [description of project objectives] which are not active, nor would be active, in the market for [functionality] analysis and

395 Synopsys internal document, SNPSCMA-00012334, […], dated 21 November 2023.
396 Synopsys internal document, […], dated of November 2023, slides 4 and 44.
397 Synopsys internal document, Annex PN RFI 4 - Q.16-015, […], dated 16 November 2023, slides 2-7.
398 Synopsys internal document, SNPSCMA-00011784, titled […], dated June 2023, slide 5, 7 and 14.
399 Synopsys submission on potential competition, para. 2.16.
400 Synopsys internal document, Annex PN RFI 4 - Q.16-014, […] dated 2024, slide 1.
401 [Synopsys internal documents].
402 Synopsys internal document, M.11481 - 4(c)-2 […], of October 23, slide 31.
403 Response to CMA Issues Letter, […].
404 [Synopsys internal documents].

compete with Ansys' [tool name], Cadence's [tool name] and Siemens' [tool name], which are the main players in this market.

(435) These capabilities will rather only allow the tools [description of project objectives], particularly [name of Synopsys' tools], to compete more closely with competing tools for [functionality] for digital chips and [functionality] for multi-die chips, i.e., respectively, with Cadence's [tools] tools and Siemens' [tools].[405]

(436) **Second**, and in addition to the absence of sufficiently concrete plans, the Commission considers that Synopsys would not have the incentives to build a [project objective] tool for [functionality] analysis in multi-die chip design with a [functionality] tool, which means that economic viability of entry in this market would be merely hypothetical, for the following reasons.

(437) In the first place, Synopsys' already relies in its partnership with Ansys to provides its customers with access to Ansys' multiphysics sign-off tools such as RedHawk(-SC), RedHawk-SC Electrothermal and HFSS. Under the partnership with Ansys, in which Synopsys [Synopsys' business strategy], it is able to meet customers' needs for these sign-off capabilities which it is not able to provide itself. `

(438) This is evidenced by internal documents assessing counterfactual scenarios which show that, absent the Transaction, Synopsys did not contemplate the development of a [functionality] analysis tool which would allow Synopsys to enter the market for [functionality] analysis and compete with Ansys' standalone sign-off tools for multi-die.

(439) In the second place, even though multi-die chip design is a main new market trend in which Synopsys has been heavily investing and innovating in this field, there is no evidence that Synopsys would have a strategic interest to enter the market for [functionality] an analysis for multi-die chip design or that such entry would be economically viable[406].

(440) *Firstly*, apart from the one internal document with reference to Project [project name] for [project objectives] – which have been analysed above – no internal documents evidence a strategic interest of Synopsys in developing a [feature] sign-off tool for [functionality] analysis for multi-die chip design.

(441) *Secondly*, while it may be, in theory, possible to further develop Project [project name] into a sign-off tool, this would require significant expertise, investment and time, as submitted by the Parties and corroborated by the feedback of market participants. For instance, a market participant explained that while "Synopsys could start developing its own multi-physics analysis tools for multi-die chip design […] [f]or a standalone Synopsys to gain significant market share, it would likely take a decade or more."[407]

(442) In this context, the Commission recalls that while Project [project name] is at a more advanced stage, having functionalities already in [development stages], Project [project name] is at a much earlier stage.

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405 Synopsys submission on potential competition, para. 2.4.

406 Form CO, para. 539 to 547.

407 Market participant's response to the European Commission's RFI 2, para. 23.2.

(443) *Thirdly*, in the event Synopsys would enter the market for [functionality] analysis for multi-die chip design, it is unclear whether it would be successful and become an effective competitor. While Synopsys has some successful sign-off tools in its portfolio (such as PrimeTime or PrimePower), it previously had a [functionality] analysis tool, [Synopsys' tool], which was moved to end-of-life stage after it failed to gain traction in the market. As previously explained, Synopsys discontinued the tool in favour of the partnership with Ansys, under which it started offering [Ansys' tool] and developed [Ansys' tool].[408]

(444) Accordingly, the Commission considers Synopsys would not have 'real and concrete possibilities' to enter the market for [functionality] analysis for multi-die chip design and to compete with established undertakings in that market.

5.3.3.4.2.4. Conclusion

(445) The Commission therefore concludes that Synopsys would not have 'real and concrete possibilities' to enter the markets for [functionality] analysis and/or [functionality] for multi-die chip design.

5.3.3.4.3. Other potential competitors are likely to maintain sufficient competitive pressure post-Transaction

(446) According to the Horizontal Merger Guidelines, there must not be a sufficient number of other potential competitors, which could maintain sufficient competitive pressure after the merger.[409] A lack of sufficient other potential competitors exerting sufficient competitive pressure post-merger can be due to various reasons, such as, for instance, the fact that no other potential competitor remains, or that the remaining potential competitors are facing significant barriers to entry which they are less likely to overcome than the target undertaking, or that the addition of the target undertaking to the acquirer's portfolio decreases the competitive pressure that would otherwise likely have been exerted by the remaining potential competitors vis-à-vis the incumbent firm.

(447) The Commission considers that the Merged Entity would continue to face actual and potential competitive pressure from Ansys' competitors in S&A, for the markets for [functionality] analysis and [functionality] tools.

5.3.3.4.3.1. [Functionality]analysis tools

(448) The Commission considers the Merged Entity would continue to face sufficient competitive pressure coming from credible alternatives in the market for [functionality] analysis, namely Cadence and Siemens, which are likely to expand, , as well as potential competition from other S&A companies.

(449) **First,** S&A companies already offer alternatives to Ansys' [product names] are likely to increase their competitive position by further expansion.

(450) In the first place, the results of the market investigation indicated that Cadence's [product name] and Siemens' [product name] are perceived as alternatives to

408 Synopsys' Letter to the FTC on […], dated 18 November 2024.

409 Horizontal Merger Guidelines, para. 60.

Ansys' [product name], as these were respectively the first and second most chosen option.[410]

(451) Cadence's [product name] offers [functionality].[411] Siemens' [product name] integrates with the [functionality] workflow as a tool for [functionality].[412] One respondent to the market investigation pointed out that [product name] "[p]*rovides robust* [functionality] *simulation, especially effective for multi-die packages where detailed* [functionality] *modeling is required*."[413]

(452) In the second place, the Commission considers Siemens' competitive position in multiphysics for multi-die chip de-sign, specifically in the market for [functionality] analysis is likely to grow, resulting in more competitive pressure to the Merged Entity.

(453) In [date] Siemens launched [product name], a specific [functionality] analysis tool for the multi-die chip design flow, offering similar functionality to Ansys' [product name]. This is an example recent expansion by Siemens of its offering in multiphysics for multi-die. The Commission considers that this tool can start gaining traction with customers as an alternative to [product name] for [functionality] analysis sign-off.

(454) In addition, Siemens has recently announced its intention to grow its capabilities through the acquisition of Altair – creating "the world's most complete AI-powered design and simulation portfolio."[414] Siemens' executives have already announced that the acquisition of Altair – the second largest deal in Siemens' history – is "definitely not the last acquisition Siemens makes in the area of software."[415] The Commission notes that Altair, a player in the S&A area, which also offers tools with [functionality] analysis capabilities ([product name]). Such transaction could reinforce Siemens position in the market [functionality] analysis.

(455) **Second**, S&A companies are better placed than Synopsys to enter and/or expand their offers in [functionality] analysis, given that barriers to entry would lower for players already active in S&A.

(456) As explained in Section 5.3.3.4.1 above, Ansys' is an S&A player offering a limited portfolio of tools for EDA, focused on multiphysics analysis for sign-off. Therefore, Ansys' main competitors are other S&A players, namely Cadence and Siemens – who are main competitors in EDA but also have extensive capabilities in multiphysics S&A tools – but also MathWorks, Dassault Systèmes, Altair, Hexagon, Keysight, among others.

(457) While the Commission has highlighted above that the development of standalone tools for multiphysics analysis for multi-die require significant expertise, investment and time, these barriers would be more easily overcome by S&A players, which are already focused on multiphysics analysis tools for a variety of

410 Replies to Questionnaire to customers and competitors of EDA and design IP, question D.A.F.1. and D.A.F.3.
411 Form CO, para. 1044.
412 Form CO, Table 53.
413 Replies to Questionnaire to customers and competitors of EDA and design IP, question D.A.F.3.1.
414 Siemens' press release of 30 October 2024, available at: Siemens strengthens leadership in industrial software and AI with acquisition of Altair Engineering | Press | Company | Siemens.
415 Form CO, para. 1047.

sectors and use cases. Therefore, such players would be better placed than Synopsys to grow and expand their offer to develop a [functionality] analysis standalone tool that would compete with the Merged Entity.

(458) This has also been confirmed by the results of the market investigation, as two competitors active in S&A tools have indicated they would "*start supplying multi-die chip design tools that would compete with Ansys' [product names]*".[416]

(459) As submitted by the Notifying Party, some of these competitors have recently started expanding their offering for multiphysics tools for multi-die chip design, specifically for (i) [functionality] analysis; and (ii) [functionality]analysis, which would compete with Ansys tools, namely for the sign-off stage, namely Siemens, Dassault, Keysight and Cadence.".417

5.3.3.4.3.2. [Functionality] analysis tools

(460) The Commission considers the Merged Entity would continue to face sufficient competitive pressure coming from credible alternatives in the market for [functionality], namely Cadence and Siemens, as well as potential competition from other S&A companies.

(461) **First**, S&A companies already offer alternatives to Ansys' tools for [functionality] for multi-die chip design and are likely to increase their competitive position by further expansion.

(462) In the first place, with regards to [functionality] analysis, the results of the market investigation confirmed that Cadence's [product name] is the main alternative to [Ansys product]. Siemens' [product name] has also been indicated as an alternative by some market participants.[418]

(463) Cadence's [product name] is used for [functionality] analysis for IC and multi-die designs and is integrated with [product names]. [Product name] also integrates Cadence's analysis capabilities, including [product name] for [functionality] analysis, [product name] for [functionality] analysis, [product name] for [functionality] analysis, [product name] for [functionality], and [product name] for [functionality]analysis.[419] Siemens' [product name] is a transistor-level and gate-level [functionality] analysis tool used for analog, digital, and multi-die chip design.[419].[420]

(464) In the second place, with regards to [functionality] analysis, the results of the market investigation indicated that Cadence's [product name] and [product name] are considered the main alternatives to Ansys' [product name], as these were respectively the first and second most chosen options. Other customers have also indicated Siemens' [product name] or Keysight's [product name].[421]

(465) Cadence's [product name] is a [functionality] tool for [functionality]. The [product name] helps designers tackle the most complex [functionality] challenges when

416 Replies to Questionnaire to competitors of EDA and design IP, question D.A.F.6.
417 Parties' response to the European Commission's RFI 25, para. 5.3.
418 Replies to Questionnaire to competitors of EDA and design IP, question D.A.C.1
419 Form CO, para. 1045 and 575.
420 Form CO, para. 586.
421 Replies to Questionnaire to customers and competitors of EDA and design IP, question D.A.F.2.

[functionality].[422] Siemens' [product name] is a family of tools offered by Siemens that are optimised for [functionality] analysis, and that include capabilities such as [functionality]. Keysight's [product name] provides [functionality] for analysing [functionality] of components.[423].[424] One respondent to the market investigation pointed out that [product name] "has direct competition in Cadence [product name] and Keysight [product name]"[425]

(466) **Second**, S&A companies are better placed than Synopsys to enter and/or expand their offers in [functionality], given that barriers to entry would lower for players already active in S&A.

(467) As explained above, Ansys' is an S&A player offering a limited portfolio of tools for EDA, focused on multiphysics analysis for sign-off. Therefore, Ansys' main competitors are other S&A players, namely Cadence and Siemens – who are main competitors in EDA but also have extensive capabilities in multiphysics S&A tools – but also MathWorks, Dassault Systèmes, Altair, Hexagon, Keysight, among others.

(468) While the Commission has highlighted above that the development of standalone tools for multiphysics analysis for multi-die require significant expertise, investment and time, these barriers would be more easily overcome by S&A players, which are already focused on multiphysics analysis tools for a variety of sectors and use cases. Therefore, such players would be better placed than Synopsys to grow and expand their offer to develop a [functionality] standalone tool that would compete with the Merged Entity.

(469) This has also been confirmed by the results of the market investigation, as two competitors active in S&A tools have indicated they would "*start supplying multi-die chip design tools that would compete with Ansys'* [product names]".[426]

(470) As submitted by the Notifying Party, some of these competitors have recently started expanding their offering for multiphysics tools for multi-die chip design, specifically for (i) [functionality] analysis; and (ii) [functionality]analysis, which would compete with Ansys tools, namely for the sign-off stage, namely Siemens, Dassault, Keysight and Cadence.[427]

5.3.3.4.4. Unlikelihood of Ansys' [Ansys' internal strategy] strategy to lead to entry in any new EDA markets for multi-die chip design

(471) As described in Section 5.3.3.4.1. above, Ansys has been pursuing a [Ansys' internal strategy] strategy, which is directed at [Ansys' internal strategy]."[428]

(472) As part of this strategy, Ansys has been working on [Ansys' internal strategy] in the market for [functionality] and [functionality], namely related to [functionality]

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422 Parties' response to the European Commission's RFI 25, para. 5.3.

423 Form CO, para. 586.

424 Parties' response to the European Commission's RFI 25, para. 5.3.

425 Replies to Questionnaire to customers and competitors of EDA and design IP, question D.A.F.3.1.

426 Replies to Questionnaire to competitors of EDA and design IP, question D.A.F.6.

427 Parties' response to the European Commission's RFI 25, para. 5.3.

428 Form CO, para. 740 and 743 and Synopsys' Reply to FTC letter on potential competition, dated 6 Decembre 2024. The goal of [Ansys' business strategy] is being executed through Ansys' [description of Ansys' business strategy and related activities].

for [product name]. In particular, Ansys has been developing [Ansys' internal strategy].[429]

(473) The Parties submit that whilst Ansys' long-term growth strategy in S&A aims to [Ansys' business strategy], these do not relate to [areas targeted by Synopsys' business strategy] Rather, Ansys is working on [Ansys's business strategy].[430]

(474) The Commission considers that Ansys [business strategy] is unlikely to lead to entry in any new functional EDA markets for multi-die chip design where Synopsys is active, for the reasons de-scribed below.

(475) **First**, the Commission considers that Ansys [Ansys' internal strategy] strategy relates solely to [product name], which is already a competitor in the market for [functionality] analysis and [functionality] for multi-die chip.

(476) In the first place, there is no evidence that Ansys' was developing [Ansys business strategy demonstrating that Ansys is not a potential competitor of Synopsys in EDA] markets. Ansys internal documents confirm that its [Ansys' internal strategy] strategy is aimed at increasing [Ansys' internal strategy] for multiphysics simulation, such as [Ansys' product name], and not directed at [Ansys' internal strategy demonstrating that Ansys is not a potential competitor of Synopsys in EDA] [431]

(477) In the second place, Ansys is already active in the markets for [functionality] analysis and [functionality] for multi-die chip design. These capabilities will be used to [product names] and would not allow these products to [Ansys' internal strategy demonstrating that Ansys is not a potential competitor of Synopsys in EDA].

(478) *Firstly*, the Commission notes that while [product name] can be run [functionality] to perform [functionality] analysis when [functionality], it still requires a full set of design parameters and runs a highly accurate yet time consuming [functionality] analysis due to the complexities and granularity of the "checks" it performs as a sign-off tool.[432]

(479) However, it is not, nor is it intended to be, [Ansys' internal strategy demonstrating that Ansys is not a potential competitor of Synopsys in EDA], as is the case of Project [Synopsys project name].

(480) *Secondly*, the use of [product name] prior to [functionality] has been developed as part of the partnership with Synopsys, under which [product name] can be [functionality]. Nonetheless, Synopsys still developed Project [project name], in view of customer demand for [capabilities] capabilities [Synopsys' business strategy], which could not be provided under the existing partnership. Accordingly, Project [project name] and Ansys' [Ansys' strategy] strategy regarding [product name] target complementary rather than competing capabilities.[433].[434].

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429 Idem.

430 Form CO, para. 740.

431 [Ansys' internal documents].

432 Annex RFI 25, Q 6.1, Parties' Reply to the FTC Letter of 21 November 2024, dated 6 December 2024.

433 Annex RFI 25, Q 6.1, Parties' Reply to the FTC Letter of 21 November 2024, dated 6 December 2024. [Ansys' business R&D initiatives].

(481) Accordingly, there are no concrete plans from Ansys to enter any new EDA markets in which it would be a competitor with Synopsys.

(482) **Second,** the Commission considers that Ansys' would not have the abilities and incentives to enter new EDA markets unrelated to multiphysics analysis, in which it would compete with Synopsys. Therefore, economic viability of entry in such markets would be merely hypothetical.

(483) In the first place, the Commission considers that Ansys does not have any specific incentives to enter any EDA markets unrelated to multiphysics analysis. Ansys is essentially an S&A player, with a limited semiconductor related portfolio, accounting for only [10-20]% of its revenues. [435]

(484) Ansys' semiconductor offering is focused on multiphysics S&A tools used at the sign-off stage. It does have tools competing with Synopsys' design tools, namely IC Compiler, Fusion Compiler and 3D-IC Compiler.[436] Ansys' product roadmaps and R&D efforts in its semiconductor business show [Ansys' business strategy], rather than entering any new EDA markets. This is corroborated by Ansys' internal documents, as mentioned above.

(485) In the second place, the Commission considers Ansys does not have the technology and R&D capabilities today required to offer EDA capabilities that would compete with Synopsys for new EDA markets unrelated to multiphysics sign-off, and could not quickly develop such technology and R&D capabilities.[437] In any case, it would take Ansys significant time and investment to be able to enter new EDA markets, regardless of whether these are related or unrelated to multiphysics sign-off tools.

(486) In light of the above, the Commission concludes that Ansys does not have any real and concrete possibilities of growing into an effective competitor of Synopsys in any new EDA markets.

5.3.3.5. Conclusion

(487) In view of the above considerations and in light of the results of the market investigation and the evidence and information available to it, the Commission concludes that the Transaction does not raise serious doubts as to its compatibility with the internal market as a result of horizontal non-coordinated effects related to the loss of potential competition from Synopsys in multiphysics analysis tools for multi-die chip design, specifically in the markets for the global supply of [functionality] analysis and [functionality] analysis, given that Synopsys is not significantly likely to grow into an effective competitive constraint in such markets. In any case, there are sufficient other potential competitors, which would maintain competitive constraints to the Merged Entity.

(488) The Commission further concludes that the Transaction does not raise serious doubts as to its compatibility with the internal market as a result of horizontal non-coordinated effects related to the loss of potential competition from Ansys, as

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434 Annex RFI 25, Q 6.1, Parties' Reply to the FTC Letter of 21 November 2024, dated 6 December 2024.

435 Form CO, para. 246.

436 Form CO, para. 736.

437 Form CO, para. 472.

Ansys' [business strategy] would not lead to entry in any new markets, but rather [goals targeted by Ansys' business strategy and R&D initiatives].

5.4. Conglomerate non-coordinated effects

(489) This Section assessing conglomerate (non-coordinated) effects is structured as follows. First, Section 5.4.1 provides an overview of the conglomerate relationships that will be assessed by the Commission. Second, Section 5.4.2 sets out the legal framework for the Commission's assessment of conglomerate effects resulting from the Transaction. Third, Section 5.4.3 describes the potential conglomerate theories of harm or foreclosure mechanisms that will be assessed. Fourth, Section 5.4.4 provides the Notifying Party's views that apply generally to all conglomerate relationships. Finally, Sections 5.4.5 to 5.4.10 proceed with the Commission's assessment of the conglomerate effects resulting from the Transaction (by the groups of conglomerate relationships outlined in Section 5.4.2).

5.4.1. Overview of conglomerate relationships

(490) The Transaction results in a number of conglomerate relationships between Synopsys' activities in certain EDA markets on the one hand and Ansys' activities in closely related EDA markets on the other hand. Both Parties supply EDA tools, albeit largely at different stages of the chip design process (commonly referred to as the design flow). Most of Ansys' EDA tools are typically used for the physical verification and sign-off analysis, which is the final stage of the design flow before sending the chip for manufacturing in the foundry. Ansys also offers a limited number of EDA tools offering specialised analysis capabilities in other stages of the design flow.[438] On the other hand, Synopsys offers a suite of EDA tools across all stages of the design flow, and in all the EDA tool categories that are essential for designing a basic digital or analog chip.[439] EDA tools interoperate in the chip design process through an import or export relationship between two EDA tools. In other words, EDA tools in one market exchange data with EDA tools in another market, thereby creating a link between two EDA markets based on interoperability.

(491) In addition, the Transaction results in a number of conglomerate relationships between Synopsys' activities in design IP markets on the one hand and Ansys' activities in the EDA markets on the other hand. Design IP products and EDA tools are considered to belong to neighbouring markets because, first, companies designing a chip need to develop or procure both design IP and EDA tools, and, second, EDA tools are also used by design IP licensors in order to develop their design IP.

(492) As indicated in Section 5.1.2, there are **36 conglomerate leveraging markets**. This includes instances where the Parties' individual or combined share exceeds 30% by revenue at the worldwide level in 2023, and where one or both Parties are active in neighbouring markets.

(493) As outlined in Section 5.4.3 below, the Commission considers **two practices** by way of which the Merged Entity could potentially leverage a strong market position in one market into another one and foreclose competitors in the latter: (i)

438 Form CO, para. 330.
439 Form CO, para. 330.

technical tying via the total restriction or degradation of interoperability, and (ii) anticompetitive (pure and/or mixed) bundling. Each of these practices therefore generates its own conglomerate relationships from the 36 conglomerate leveraging markets.

(494) **With respect to technical tying via the total restriction or degradation of interoperability**, only 26 of the 36 conglomerate leveraging markets are relevant, since the other 10 conglomerate leveraging markets do not have any interoperability links with other products of the Parties.[440] As described in Annex A of this Decision, for the purpose of identifying the relevant interoperability links, the Commission requested the Parties to complete an interoperability matrix identifying data export-import relationships between EDA tools and design IP markets for each EDA function where one or both of the Parties generated revenues in 2023.[441]

(495) As outlined in Table 42, these 26 conglomerate leveraging markets correspond to 149 conglomerate relationships based on interoperability links ("affected interoperability pairings").[442] [443] As indicated in Table 42 below, Ansys is solely active in 6 conglomerate leveraging markets (corresponding to 47 affected interoperability pairings), Synopsys is solely active in 16 conglomerate leveraging markets (corresponding to 75 affected interoperability pairings), and both Synopsys and Ansys are active in 4 conglomerate leveraging markets (corresponding to 27 affected interoperability pairings).

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440 An interoperability link means there is a possible import or export relationship between two markets, i.e., that EDA tools in one market exchange data with EDA tools in another market, thereby creating a link between two markets based on interoperability. As a result, an EDA tool may be preceding or succeeding other EDA tools in the design flow.

441 See Annex A of this Decision that shows the export-import relationships for each EDA function. Table 10 of Annex A also shows which relationships are affected from a conglomerate perspective at the functional level. That is, whether the Parties' combined market share in either the exporting or importing function is at least 30%, or whether one of the Parties' market share in either the exporting (or importing) function is at least 30% and the other Party is present in the importing (or exporting) function.

442 Because most of the conglomerate leveraging markets import/export data to/from more than one market in which the other Party is active, there are significantly more than 26 interoperability pairings resulting from the 26 conglomerate leveraging markets.

443 The 149 interoperability pairings include instances where a conglomerate leveraging market is linked to another conglomerate leveraging market. In such instances, these interoperability pairings are counted twice (once for each direction). For example, gate-level power integrity analysis has an interoperability link with RTL power consumption analysis, and both of these markets are conglomerate leveraging markets. Therefore, this interoperability link is counted twice within the 90 interoperability pairings (once under each market), in order to account for the different leveraging directions, i.e., leveraging from gate-level power integrity analysis into RTL power consumption analysis, as well as leveraging from RTL power consumption analysis to gate-level power integrity analysis.

Table 42: Conglomerate relationships based on interoperability links

Industry	Conglomerate leveraging market	Parties' activities	Market share by revenue in 2023	Total market size (USD m)	Total number of corresponding interoperability pairings
EDA	Gate-level power integrity analysis	Ansys	[50-60]%	[…]	17
EDA	Gate-level security analysis	Ansys	[90-100]%	[…]	12
EDA	Structural and thermal analysis	Ansys	[70-80]%	[…]	4
EDA	Clock jitter analysis	Ansys	[50-60]%	[…]	8
EDA	Electromagnetic simulation	Ansys	[50-60]%	[…]	4
EDA	Signal and power integrity	Ansys	[30-40]%	[…]	2
EDA	Parasitic analysis	Both	[70-80]%	[…]	5
EDA	Power device analysis	Both	[40-50]%	[…]	6
EDA	RTL power consumption analysis	Both	[70-80]%	[…]	7
EDA	Transistor-level power integrity analysis	Both	[40-50]%	[…]	9
EDA	RTL analysis	Synopsys	[90-100]%	[…]	1
EDA	Timing analysis	Synopsys	[80-90]%	[…]	4
EDA	Design robustness	Synopsys	[80-90]%	[…]	2
EDA	ECO	Synopsys	[80-90]%	[…]	2
EDA	Debug verification	Synopsys	[70-80]%	[…]	1
EDA	Gate-level power consumption analysis	Synopsys	[70-80]%	[…]	3
EDA	RTL synthesis	Synopsys	[60-70]%	[…]	1
EDA	Parasitic extraction	Synopsys	[40-50]%	[…]	9
EDA	Characterisation	Synopsys	[40-50]%	[…]	4
EDA	Place and route	Synopsys	[40-50]%	[…]	4
EDA	Hardware-assisted verification	Synopsys	[40-50]%	[…]	1
EDA	Simulation verification	Synopsys	[40-50]%	[…]	4
EDA	Circuit simulation	Synopsys	[30-40]%	[…]	13
Design IP	Embedded memories	Synopsys	[50-60]%	[…]	10
Design IP	Physical libraries	Synopsys	[30-40]%	[…]	10
Design IP	Wired interface IP	Synopsys	[60-70]%	[…]	6

(496) **With respect to anticompetitive (pure and/or mixed) bundling**, the 36 conglomerate leveraging markets correspond to a very high number of closely related neighbouring markets with which the Parties could bundle their products. Many EDA tools, as well as design IP, are purchased by the same set of customers (either together or separately) to perform complementary tasks. Therefore, many EDA tools in the chip design flow, as well as design IP, are interrelated and complementary in nature, and thereby could potentially be sold together in a bundle. As such, given the high number of products offered by both Parties, the 36 conglomerate leveraging markets generate a very high number of conglomerate relationships based on potential bundling ("bundle pairings"). In addition to the conglomerate leveraging markets in Table 42 above, Table 43 below lists the 10 additional conglomerate leveraging markets relevant for potential bundling. Synopsys is solely active in these 10 additional markets.

Table 43: Conglomerate relationships based solely on potential for bundling

Industry	Conglomerate leveraging market	Parties' activities	Market share by revenue in 2023	Total market size (USD m)	Total number of corresponding interoperability pairings
EDA	Virtual prototyping	Synopsys	[80-90]%	[…]	0
EDA	TCAD	Synopsys	[80-90]%	[…]	0
EDA	Static verification	Synopsys	[60-70]%	[…]	0
EDA	Equivalence checking	Synopsys	[30-40]%	[…]	0
EDA	FPGA Synthesis	Synopsys	[50-60]%	[…]	0
EDA	Silicon lifecycle management IP	Synopsys	[50-60]%	[…]	0
EDA	Timing constraints	Synopsys	[40-50]%	[…]	0
EDA	Design-for-test/Test IP	Synopsys	[30-40]%	[…]	0
EDA	HAT	Synopsys	[90-100]%	[…]	0
EDA	Synthesis	Synopsys	[30-40]%	[…]	0

5.4.2. Legal framework

(497) According to the Non-Horizontal Guidelines, in most circumstances, conglomerate mergers do not lead to any competition problems.[444]

(498) However, the Non-Horizontal Guidelines recognise that the main concern in the context of non-horizontal concentrations is that of foreclosure. In particular, foreclosure effects may arise when the combination of products in related markets may confer on the merged entity the ability and incentive to leverage a strong market position from one market to another closely related market by means of tying (including by restricting or degrading interoperability) or bundling or other

444 Non-Horizontal Guidelines, paragraph 92.

exclusionary practices.[445] While tying and bundling have often no anticompetitive consequences, in certain circumstances such practices may lead to a reduction in actual or potential competitors' ability or incentive to compete. This may reduce the competitive pressure on the merged entity allowing it to increase prices.[446]

(499) In assessing the likelihood of such a scenario, the Commission examines, first, whether the merged firm would have the ability to foreclose its rivals,[447] second, whether it would have the economic incentive to do so[448] and, third, whether a foreclosure strategy would have a significant detrimental effect on competition, thus causing harm to consumers.[449] In practice, these factors are often examined together as they are closely intertwined.

(500) In order to be able to foreclose competitors, the merged entity must have a significant degree of market power, which does not necessarily amount to dominance, in one of the markets concerned. The effects of bundling or tying can only be expected to be substantial when at least one of the merging parties' products is viewed by many customers as particularly important and there are few relevant alternatives for that product.[450] Further, for foreclosure to be a potential concern, it must be the case that there is a large common pool of customers, which is more likely to be the case when the products are complementary.[451] Finally, bundling is less likely to lead to foreclosure if rival firms are able to deploy effective and timely counter-strategies, such as single-product companies combining their offers.[452]

(501) The incentive to foreclose rivals through bundling or tying depends on the degree to which this strategy is profitable.[453] Bundling and tying may entail losses or foregone revenues for the merged entity.[454] However, they may also allow the merged entity to increase profits by gaining market power in the tied goods market, protecting market power in the tying good market, or a combination of the two.[455]

(502) It is only when a sufficiently large fraction of market output is affected by foreclosure resulting from the concentration that the concentration may significantly impede effective competition. If there remain effective single-product players in either market, competition is unlikely to deteriorate following a conglomerate concentration.[456] The effect on competition needs to be assessed in light of countervailing factors such as the presence of countervailing buyer power

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445 'Bundling' usually refers to the way products are offered and priced by the merged entity. Pure bundling refers to situations where the products are only sold jointly in fixed proportions. Mixed bundling refers to situations where the products are also available separately, but the sum of the stand-alone prices is higher than the bundled prices. Tying refers to situations where customers that purchase one good (the tying good) are required also to purchase another good from the producer (the tied good). Tying can take place on a technical or contractual basis. Non-horizontal Merger Guidelines, paragraphs 96-97.

446 Non-Horizontal Guidelines, paragraphs 91 and 93.

447 Non-Horizontal Merger Guidelines, paragraphs 95 to 104.

448 Non-Horizontal Merger Guidelines, paragraphs 105 to 110.

449 Non-Horizontal Merger Guidelines, paragraphs 111 to 118.

450 Non-Horizontal Merger Guidelines, paragraph 99.

451 Non-Horizontal Merger Guidelines, paragraph 100.

452 Non-Horizontal Merger Guidelines, paragraph 103.

453 Non-Horizontal Merger Guidelines, paragraph 105.

454 Non-Horizontal Merger Guidelines, paragraph 106.

455 Non-Horizontal Merger Guidelines, paragraph 108.

456 Non-Horizontal Merger Guidelines, paragraph 113.

or the likelihood that entry would maintain effective competition in the upstream or downstream markets.[457]

(503) Based on the legal framework set out above and for the purposes of this Decision, the Commission will undertake an assessment of the conglomerate relationships identified in Section 5.4.1 above in groups of the conglomerate relationships as specified further below. Given the very high number of bundle pairings, in addition to the 149 interoperability pairings, it would be unrealistic to assess each conglomerate relationship separately.

(504) The conglomerate relationships are primarily grouped by the conglomerate leveraging market from which the Merged Entity would leverage its market position (i.e., the 36 conglomerate leveraging markets outlined in Tables 42 and 43 above), and the Commission will assess all conglomerate relationships corresponding to that conglomerate leveraging market together. In each case, the Commission's assessment applies generally to all conglomerate relationships that have been grouped together (unless stated otherwise).

(505) **With respect to leveraging from Ansys' EDA tools**, the Commission first assesses separately two conglomerate leveraging markets where a conglomerate concern seems most likely (based on concerns expressed by market participants, as well as the market position of the Parties in these markets). Section 5.4.5 first assesses whether the Merged Entity would have the ability and incentive to leverage Ansys' potentially strong position in a global market for *gate-level power integrity analysis* (with its tool RedHawk(-SC)) into neighbouring EDA markets (based on both interoperability pairings and bundle pairings) where Synopsys is active, and whether such a foreclosure strategy would have a significant detrimental effect on competition in the relevant markets. Section 5.4.6 carries out a similar assessment for the Merged Entity's ability and incentive to leverage Ansys' potentially strong position in a global market for *electromagnetic simulation* (with its tool HFSS) into neighbouring EDA markets (based on both interoperability pairings and bundle pairings). Finally, Section 5.4.7 carries out a similar assessment for the Merged Entity's ability and incentive to leverage Ansys' potentially strong position in *the eight other conglomerate leveraging (EDA) markets* (and where conglomerate concerns seem less likely) into neighbouring EDA markets (based on both interoperability pairings and bundle pairings).[458] This group also includes the four conglomerate leveraging markets where both Synopsys and Ansys are active (see Table 42 in Section 5.4.1).

(506) **With respect to leveraging from Synopsys' EDA tools**, Section 5.4.8 assesses whether the Merged Entity would have the ability and incentive to leverage Synopsys' potentially strong position in the *conglomerate leveraging EDA markets* into neighbouring EDA markets where Ansys is active (based on both interoperability pairings and bundle pairings), and whether such a foreclosure strategy would have a significant detrimental effect on competition in the relevant markets. This group also includes the four conglomerate leveraging markets where both Synopsys and Ansys are active (see Table 42 in Section 5.4.1).

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457 Non-Horizontal Merger Guidelines, paragraph 114.

458 Specifically, the markets for (i) gate-level security analysis, (ii) clock jitter analysis, (iii) parasitic analysis, (iv) power device analysis, (v) RTL power consumption analysis, (vi) transistor-level power integrity analysis, (vii) structural and thermal analysis, and (viii) signal and power integrity analysis.

(507) **With respect to leveraging concerns related to design IP products,** Section 5.4.9 assesses whether the Merged Entity would have the ability and incentive to leverage Synopsys' potentially strong position in the *conglomerate leveraging design IP markets* into neighbouring EDA markets (based on bundle pairings) where Ansys is active, and whether such a foreclosure strategy would have a significant detrimental effect on competition in the relevant markets. Section 5.4.10 provides a similar assessment of the Merged Entity's ability and incentive to leverage Ansys' potentially strong position in conglomerate leveraging EDA markets into neighbouring design IP markets[459] (based on bundle pairings) where Synopsys is active.

(508) The Commission's investigation of plausible conglomerate effects of the Transaction does not concern other unaffected leveraging markets (either EDA markets or design IP markets) given that the Parties' individual or combined share in those markets is limited, i.e. below 30% by revenue in 2023, and where accordingly competition concerns are unlikely to arise. By reason of the Parties' limited market share on these markets, the Commission finds it unlikely that the Transaction would raise serious doubts as to the compatibility of the Transaction with the internal market as a result of the Parties' activities in the leveraging markets.

5.4.3. Overview of the practices that the Merged Entity could use to leverage a strong market position in one market into a neighbouring market and thereby foreclose its competitors

(509) With respect to the potential conglomerate theories of harm to be assessed, the Commission considers **two practices** by way of which the Merged Entity could potentially leverage a strong market position, as indicated in Section 5.4.2 above: Section 5.4.3.1 describes the total restriction or degradation of interoperability (technical tying) and Section 5.4.3.2 describes anticompetitive pure or mixed bundling.

5.4.3.1. Total restriction or degradation of interoperability (technical tying)

5.4.3.1.1. Introduction to interoperability between EDA tools, and between design IP and EDA tools

(510) Interoperability between EDA tools, as well as between design IP and EDA tools, is a requirement for EDA tools to properly function throughout the chip design process. Interoperability enables EDA tools to read input from design IP and other EDA tools and send output that can be read by other EDA tools in the chip design flow. To design a chip, customers need to use various design IP blocks as well as multiple EDA tools across different functions. For instance, designing a basic digital chip requires at least five functions, while designing a complex digital chip requires up to twenty functions. Interoperability is particularly important for design IP and EDA customers as they generally do not rely on a single vendor's tools for an entire chip design flow but mix-and-match tools from different vendors across the design flow. In the same vein, Synopsys design IP and the Parties' EDA tools are used alongside their respective competitors' EDA tools. Sometimes, customers also multi-source EDA tools for the same EDA functionality (i.e. "multi-home"), and thus have a policy of using at least two vendors for a certain type of EDA tool.

459 As defined in Section 4.3 above.

Therefore, interoperability ensures that each tool works with an adjacent tool in the design flow, particularly in such cases when a customer supplies EDA tools from different EDA vendors.

(511) There are different ways in which design IP licensors and EDA vendors ensure interoperability. **In the first place**, interoperability between design IP and EDA tools as well as between EDA tools is achieved primarily through industry standards ("baseline" interoperability). Baseline interoperability may be supplemented by interoperability agreements between EDA vendors for testing and bug-fixing support or automating the flow of data between EDA tools. **In the second place**, EDA vendors may conclude interoperability agreements for developing proprietary file formats and/or application programming interfaces ("APIs"). **In the third place**, an EDA vendor can natively integrate its EDA tools. Irrespective of the interoperability type, interoperability is mainly enabled through interfaces such as industry standard languages and file formats and APIs.

(512) Each type of interoperability will be described in more detail in the following paragraphs.

Baseline interoperability

(513) Nearly all design IP and EDA tools interoperate through industry-based standard interfaces, considered as a "baseline" interoperability. Baseline interoperability generally does not require approval from other design IP licensors or EDA vendors or their mutual agreements. Interoperability is presumed between two EDA tools, as well as between a design IP product and an EDA tool, that support industry-standard interfaces. Industry standard interfaces refer to file formats, design languages, and APIs that are most commonly defined and managed by standard bodies, with wide participation of stakeholders in the EDA, respectively design IP, sector including vendors, foundries and EDA customers. Industry-standard interfaces may also be defined and managed by companies as open source (provided through an open-source license). Therefore, EDA vendors can freely access industry standard interfaces without entering into a partnership agreement with other EDA vendors.[460] The same is true for design IP licensors.[461] Standard bodies provide the necessary documentation to an EDA vendor to achieve baseline interoperability and are in charge of updating the standards to ensure stability and predictability. Open-source interfaces are managed by a company, and technical documentation is provided once the EDA vendor accepts the open-source license agreement.[462] When industry standards are updated, design IP licensors and EDA vendors will update their solutions to the latest standard as needed.

(514) Baseline interoperability may be supplemented by interoperability agreements between EDA vendors for the purpose of testing and bug-fixing. As a matter of principle, EDA vendors ensure baseline interoperability through unilateral checks on their own EDA tools without any interoperability agreement. However, design IP licensors and EDA vendors occasionally require access to third-party tools to test tool compatibility and their respective implementation of industry standards, as

460 In certain cases, the EDA vendor may need to join the relevant standards body or accept an open-source license.

461 Response to Commission request for information 25 of 3 December 2024, questions 30-32.

462 For instance, on Synopsys' website, anyone can download the Interconnect Technology Format Specification after agreeing to the terms and conditions of the open source ITF License Agreement.

well as to raise technical support questions and to report a bug if an interoperability issue is found. Based on the interoperability agreements, EDA vendors cross-license their EDA tools free of charge for this purpose. These agreements are concluded either in reaction to customers identifying issues that need to be resolved or pre-emptively to prevent potential interoperability issues (e.g. when the implementation of industry-standard file format is not well established for the interaction between the given EDA tools).

(515) Interoperability agreements may also be used to support baseline interoperability by automating the relevant interoperability "flow" between EDA tools. Automating the interoperability implies converting the proprietary file format an EDA tool outputs to an industry-standard file format that can be imported by another EDA tool.

(516) Baseline interoperability is vendor-agnostic as it applies to all vendors of a given design IP product and EDA tool that complies with given industry standards. In addition, baseline interoperability is not customer-specific. Any customer using the design IP product and EDA tool that complies with a given industry standard benefits from this type of interoperability. The same principle applies also to interoperability agreements that supplement baseline interoperability.

Proprietary interoperability

(517) EDA vendors may develop proprietary interfaces (file formats and/or APIs) to improve the efficiency and speed of interoperability between specific EDA tools.[463] Given the IP rights associated with proprietary file formats and APIs and the need to license the relevant party's EDA tools to perform the required tests, proprietary interoperability is determined through interoperability agreements. The agreements are concluded either at the initiative of EDA vendors or more commonly at the request of their customers, for a specific EDA tools pairing (referred to as interoperability "flow"). Developing, testing, documenting and supporting proprietary interoperability flows entails engineering efforts for EDA vendors, who assess customer demand against the required technical effort.

(518) Compared to baseline interoperability, proprietary interfaces only improve the user experience the quality of the analysis while the delivery of results is the same. Further, in contrast to baseline interoperability, interoperability based on proprietary interfaces is vendor-specific as it applies to specific EDA tools of the EDA vendors concluding the interoperability agreement. However, it is generally customer-agnostic as any customer using the specific EDA tool pairing will benefit from interoperability established through proprietary interfaces.

(519) As a rule, even when interoperability between EDA tools is established through proprietary interfaces, an equivalent industry-standard file format exists as an alternative. Proprietary file formats generally co-exist with industry-standard file formats, i.e. in most cases the same tools can perform the same analysis through an industry-standard file format as they do with proprietary file formats. In only

463 Synopsys owns a proprietary file format called Fast Signal Database ("FSDB"), which is a proprietary version of an industry-standard file format VCD. Synopsys provides APIs to third parties to read and write FSDB. These APIs are proprietary and offered to other EDA vendors after signing interoperability agreements. This standard is widely used in the EDA industry for its efficiency and compatibility with various design and verification tools. Form CO, para. 237.

exceptional circumstances, proprietary file formats may be the only interface and there may not be an industry-standard alternative that allows for the same analysis. This is for instance the case when a link between two EDA functions is recent or is used only by a limited set of customers.[464]

Native integration

(520) Native integration establishes a different connection between EDA tools compared to baseline- and proprietary interoperability where interfaces are built between still-separate EDA tools. Developing a native integration between EDA tools entails combining those products at a source code level. When natively integrated, the EDA functionalities are delivered in a single product's source code, as opposed to two or more separate products. As the source code underlying their EDA tools is a critical asset for each EDA vendor, they are not willing to share it with competing EDA vendors even under partnership agreements due to IP expropriation risks. Therefore, native integration is realistic only between EDA tools of a single EDA vendors. Unlike proprietary interoperability that generally only improves user experience, native integration of EDA tools improves the quality of the analysis and results delivered.[465]

5.4.3.1.2. Importance of interoperability in the EDA industry

(521) The Commission will now consider the importance of interoperability in the EDA industry and for the chip design process, as well as the role of market participants (EDA vendors and their customers alike) in establishing and maintaining effective interoperability.

(522) **First**, the Commission notes that due to the characteristics of supply and demand in the EDA markets, interoperability is an important element in the EDA industry.

(523) In the first place, in principle customers purchase EDA tools from various EDA vendors in their chip design project. While some EDA providers such as Synopsys, Cadence and Siemens provide a wide portfolio of EDA tools, no EDA vendor supplies all possible functionalities that a customer might potentially need. Consequently, customers generally do not rely on a single vendor for all their EDA tools but mix-and-match EDA tools from different vendors. For instance, in 2023, customers representing ~[a significant percentage] of Synopsys' sales mixed and matched EDA tools from different vendors.[466] In providing input to the market investigation, one customer explained that "*For instance, we use one vendor for schematic capture, one for logical synthesis, one for physical [sic] integration, and one for design validation/simulation*", and another customer concluded that "*Because I take multi-vendor strategy. Interoperability between the different EDA tools is important for a seamless operation*".[467]

(524) Different EDA vendors have different strengths and weaknesses in EDA markets and the customers are mainly driven by their demand for "best of breed" tools. The majority of customers providing their views confirmed that they mix-and-match EDA tools of different vendors primarily because they ultimately want to choose

464 Parties' Paper on the Lack of Interoperability Concerns, para. 22.

465 Response to Commission request for information 25 of 3 December 2024; Parties' Paper on the Lack of Interoperability Concerns.

466 Parties' response to the European Commission's RFI 12, para. 9.2.

467 Replies to Questionnaire to customers of EDA and design IP, question C.B.1.1.

the best quality tools. When rating the parameters impacting customers' purchasing strategy and choice of EDA tools, 73% customers rated "Quality" as the most important (5/5) parameter.[468] . For instance, one customer submitted that "*[...] diversity for its own is not our goal, but a consequence from aiming at best-in-class software for particular tasks to optimize in a holistic manner.*".[469] Another customer explained that "*For sign-off and design we use tools from different vendors, since it is essential to have a 'gold standard' for sign-off tools [...]*".[470] Therefore, in choosing their EDA tools, customers will primarily be guided by their quality and in consequence use the tools of different vendors rather than purchasing a suite of tools from a single vendor.

(525) Since customers generally do not rely on a single EDA vendor, they greatly value interoperability between EDA tools they purchase. For instance, when rating the parameters impacting their purchasing strategy and choice of EDA tools, more than half of customers rated interoperability of a given EDA tool with third-party tools as the most important (5/5) and second most important (4/5).[471] In that regard, one customer explained that "*Interoperability is quite important, especially in a multi-vendor environment, as it allows for greater flexibility and integration across different tools*."[472] Another customer explained that "*Interoperability is important because we purchase EDA tools from multi-vendors*".[473] Finally, the results of the market investigation shows that this is the case irrespective of the type of chip customers are designing.[474]

(526) In the second place, the Commission notes that even in instances where they offer integrated EDA solutions comprising several tools, EDA vendors also offer the same tools on a standalone basis because their customers are keen to mix and match EDA tools of their choice. For instance, Synopsys offers Fusion Compiler, an EDA suite solution, which integrates synthesis (Design Compiler), place & route (IC Compiler II), and extraction (StarRC) tools' capabilities, while keeping all these tools separately available for customers to combine with EDA tools of other vendors. As regards Ansys, all of its tools are available to customers on a standalone basis.[475] The fact that EDA vendors generally (also) offer their tools on a standalone basis to address customer demand appears also to be instructive of their incentive to maintain effective interoperability with tools of a competing vendor.

(527) In the third place, effective interoperability is an important element in the EDA tool certification provided for by the foundries. For EDA tools that are used for the sign-off stage of the chip design (such as RedHawk(-SC)), customers typically demand their certification by one or more foundries (i.e., they demand them to be "foundry-certified"). As part of their certification process, foundries will also evaluate how EDA tools work with one another and how this impacts the overall accuracy and effectiveness of the design flow. As such, the foundry will only provide the certification when a sufficiently high level of interoperability exists

468 Replies to Questionnaire to customers of EDA and design IP, question C.A.1.
469 Replies to Questionnaire to customers of EDA and design IP, question C.A.2.
470 Replies to Questionnaire to customers of EDA and design IP, question C.B.1.1.
471 Replies to Questionnaire to customers of EDA and design IP, question C.A.1.
472 Replies to Questionnaire to customers of EDA and design IP, question C.A.2.
473 Replies to Questionnaire to customers of EDA and design IP, question C.A.2.
474 Replies to Questionnaire to customers of EDA and design IP, question C.A.2.
475 Parties' response to the European Commission's RFI 22, para. 21.4.

between the EDA tool of a given vendor and other EDA tools, including from other vendors. As Intel explained, '*This sort of certification is also proof of EDA tool interoperability being the standard in the EDA market(s).*'[476]

(528) **Second**, because of its importance, interoperability is a widely adopted practice and EDA vendors generally work extensively on establishing and maintaining interoperability with EDA tools of their competitors.

(529) In the first place, the Commission notes that all Synopsys' products supporting interoperability with third party tools are based on either industry-standard interfaces or proprietary interfaces.[477] In addition to maintaining baseline interoperability, Synopsys has a large number of collaborations with competing EDA vendors and other third parties in the form of interoperability agreements supporting baseline interoperability or proprietary interfaces. Synopsys has around [a significant number] supported interoperability flows with its two closest competitors Cadence […]) and (Siemens, approx. […]). Synopsys also supports interoperability flows with other EDA vendors, such as Keysight ([…]), Lorentz ([…]), and Zuken ([…]), as well as interoperability agreements with other competitors such as MathWorks, Altair and Dassault.[478]

(530) In the second place, EDA vendors such as Synopsys, Cadence and Siemens support industry-based standard interfaces with rival EDA tools, even for their market leading EDA tools. For instance, Synopsys' PrimeTime (a timing analysis tool with [80-90]% market share by revenue worldwide in 2023), interoperates with Siemens' gate-level power integrity analysis tool mPower based on industry standards as well as proprietary interfaces.[479] Similarly, Cadence's Innovus (a place & route tool with [50-60]% market share by revenue worldwide in 2023), and Siemens' Calibre (a physical verification tool with [60-70]% market share by revenue worldwide in 2023), interoperate with rival EDA tools based on industry-standard formats.[480]

(531) **Third**, customers have a significant role in demanding and maintaining effective interoperability.

(532) In the first place, based on the review of the Notifying Party's internal documents, the Commission notes that customers may demand and put pressure on EDA vendors to enhance interoperability and/ or implement interoperability agreements to that end.[481] For instance: [examples of customer requests for interoperability between specific tools].[482] .[483] .[484].[485]

(533) In the second place, the market investigation showed that interoperability is strongly driven by EDA customers. At least a third of customers requested EDA vendors to conclude interoperability agreements in the past. Customers request

476 Minutes of a call with a market participant dated 24 June 2024, para. 16.
477 Form CO, para. 1052
478 Form CO, para. 1072.
479 Parties' response to the European Commission's RFI 22, Table 3.
480 Parties' Paper on the Lack of Interoperability Concerns, para. 13.
481 Parties' response to the European Commission's RFI 22, para. 14.2.
482 Form CO, Annex PN RFI 22 Q. 14.001.
483 Form CO, Annexes PN RFI 22 Q. 14.002-3.
484 Form CO, Annex PN RFI 22 Q. 14.004.
485 Form CO, Annex PN RFI 22 Q. 14.005.

interoperability so they can mix and match EDA tools of different vendors and purchase the 'best of breed' EDA tools for their specific chip design project. In addition, many customers providing views to the market investigation explained that they expect interoperability between EDA tools and EDA vendors to maintain it, even without requesting an interoperability agreement. For instance, one customer explained that "*If tool interfaces and/or tool integrations break, then EDA vendors point to each other as cause of the problem, leaving the customer dealing with the actual problem. We therefore request critical interfaces to be maintained*." One customer explained that while it has not pursued written agreements from EDA vendors, it "*has worked with various EDA providers to achieve [interoperability] on a case-by-base basis*.", and another customer explained that "*currently, there are no specific interoperability agreements in place but there is an expectation that interoperability is available and remains secured*." Another customer explained that "*No specific request has been made to conclude any interoperability agreements as the norm is that EDA tools are generally interoperable […]*."[486]

(534) In the third place, customers regularly insist that EDA vendors support interoperability even for EDA tools that are sold in integrated EDA solutions. For instance, the Notifying Party's internal documents show that [examples of customer requests for interoperability between Synopsys tools and other EDA vendor tools].[487] .[488]

(535) In the fourth place, the customers' demand for interoperability generally limits EDA vendors' ability and incentive to reject customers' requests for interoperability. Based on the experience of most customers expressing their view in the market investigation, EDA vendors never denied their request to conclude an interoperability agreement with a competing EDA vendor.[489]

5.4.3.1.3. Outline of potential practices involving the total restriction or degradation of interoperability

(536) In the light of the foregoing considerations, the Commission has considered several potential practices of total restriction or degradation of interoperability in which the Merged Entity could engage to potentially leverage a strong market position in one market into another one and foreclose competitors in the latter. The potential theories of harm described below concern the total restriction or degradation of interoperability that presently exists between the Merged Entity's design IP and EDA tools, and the EDA tools of their competitors based on either industry standards and/or proprietary interfaces.

(537) In that respect, the Commission notes that as part of the Transaction rationale, Synopsys is planning to *natively* integrate some of Ansys' EDA tools into Synopsys' EDA tools (for more details, see Section 5.3.3.4.1 above). As explained in Section 5.4.3.1.1 above, native integration is different from interoperability *stricto sensu*. Native integration combines EDA tools at the source code level, such that they deliver their capabilities as a one single product. Sharing a source code of

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486 Replies to Questionnaire to customers of EDA and design IP, question C.B.1.1.

487 Annexes PN RFI 22 Q.14.002-3.

488 Parties' Paper on the Lack of Interoperability Concerns, para. 20. Parties' response to the European Commission's RFI 22, Annexes PN RFI 22 Q.14.002-3.

489 Replies to Questionnaire to customers of EDA and design IP, question C.B.2.

their EDA tools to natively integrate is generally not possible between EDA competitors due to the risk of IP expropriation. Native integration is therefore only realistic for EDA tools of the same vendor. Indeed, the Commission notes that Ansys has not planned to establish native integration with other EDA vendors absent the Transaction. Presently, Synopsys' and Ansys' design IP and EDA tools interoperate with their competitors' EDA tools only based on industry standards (primarily) and proprietary interfaces (to a lesser extent) developed through partnership agreements. The Commission's assessment will therefore focus on whether the Transaction could change the *existing* interoperability between the Merged Entity's and rival EDA tools, by hampering (i.e. totally restricting or degrading) interoperability based on industry standards and/or proprietary interfaces. Consequently, the future native integration between the Parties' products will not be considered in the context of potential theories of harm involving the total restriction or degradation of interoperability.

(538) The Commission has considered several potential practices of total restriction or degradation of an interoperability that presently exists between the Merged Entity's design IP and EDA tools, and the EDA tools of their competitors.

(a) **First**, the Merged Entity could in theory totally restrict or degrade interoperability based on proprietary interfaces. This could occur by for instance terminating existing interoperability agreements or degrading or delaying the engineering work required for developing, testing, documenting and supporting proprietary interoperability based on existing interoperability agreements. The Commission notes that a total restriction or degradation of proprietary interoperability does not necessarily mean that EDA tools cannot interoperate at all. As a rule, even when interoperability between EDA tools is established through proprietary interfaces, an equivalent industry-standard file format exists as an alternative to proprietary interfaces. While proprietary interoperability agreements are common in the industry, different EDA vendors' tools can work together based on industry standards without an interoperability agreement. However, there are exceptions. If the Merged Entity has a significant degree of market power with the product whose proprietary interoperability it selectively restricts or degrades, and if interoperability based on proprietary interfaces is an important consideration for customers, then its termination or degradation may potentially allow the Merged Entity to foreclose competitors.

(b) **Second**, the Merged Entity could totally restrict or degrade interoperability based on industry standards (i.e. baseline interoperability). This degradation of interoperability could occur by for instance refusing to sell Merged Entity's products standalone and providing them only as integrated; by terminating or degrading their compliance with industry standards while making their products work based only or primarily on proprietary faces; or by refusing to complete their obligations under existing interoperability agreements that supplement baseline interoperability. As outlined in Section 5.4.3.1.1 above, baseline interoperability is generally achieved without any interoperability agreement and occasionally supplemented by interoperability agreements providing for testing and debugging support. If the Merged Entity has a significant degree of market power for a given tool and selectively restricts or degrades its baseline interoperability, and/or if interoperability agreements supplementing baseline interoperability are an important consideration for customers, then their termination or degradation may potentially allow the merged entity to foreclose competitors.

(539) In that respect, some market participants have raised concerns that the merged entity could leverage market power in several EDA markets to foreclose competing providers of EDA software tools by totally restricting or degrading interoperability between the products in different ways.

(a) For instance, one market participant noted that the Merged Entity could restrict interoperability by terminating existing interoperability agreements. Interoperability agreements are typically very short-term, lasting between 3 months and 1 year. According to that market participant, interoperability agreements may be terminated with 30 days' notice, which will enable the Merged Entity to restrict interoperability between Ansys' EDA tools and rival EDA tools. In addition to terminating interoperability agreements, the market participant considered that the Merged Entity could also degrade interoperability by making code adjustments that make the interoperability between the Merged Entity's tools and third-party tools more difficult or cumbersome. In addition, the Merged Entity could introduce new proprietary interfaces that would only support the Merged Entity's EDA tools but not competitors' EDA tools.[490]

(b) Another market participant considered that Ansys has consistently ensured that their tools can seamlessly interoperate with third-party tools, while Synopsys has a documented history of (i) delaying, (ii) degrading or (iii) entirely removing interoperability with its standalone tools, which shows its ability to do so with Ansys' EDA tools post-Transaction.[491] For instance, with respect to delaying interoperability, the market participant noted that Synopsys has in the past first released innovative features within the integrated version of its EDA tools, and only made these features available as a standalone version a year or more later. Such practices drive customers towards the integrated version to get the most recent features.[492] With respect to degrading interoperability, the market participant pointed out specific quality issues that had arisen in interoperability between Synopsys' and third-party's EDA tools.[493] Finally, the market participant noted that Synopsys has restricted interoperability with EDA tools following its past acquisitions, by refusing to sell the acquired EDA tool standalone and integrating its in its own product offering.[494]

(c) Another market participant expressed concerns that, post-Transaction, the Merged Entity could delay or degrade interoperability with third-party EDA tools, and that it would be extremely costly for the market participant to switch to alternative tools in response to such strategy.[495] According to the market participant, the Merged Entity would focus on improving interoperability between Ansys' and Synopsys' products, while degrading interoperability with third-party products by for instance delaying certain new features.[496]

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490 Market participant's response to the CMA's Questionnaire of 21 October, question 6.
491 Market participant's submission to the European Commission dated 14 June 2024, paras 122-125.
492 Market participant's submission to the European Commission dated 14 June 2024, para. 123.
493 Market participant's submission to the European Commission dated 14 June 2024, para. 124.
494 Market participant's submission to the European Commission dated 14 June 2024, para. 125.
495 Replies to Questionnaire to customers of EDA and design IP, question D.B.C.2.1.
496 Replies to Questionnaire to customers of EDA and design IP, question D.B.C.7.

5.4.3.2. Anticompetitive (pure and/or mixed) bundling

(540) With regard to bundling, the Merged Entity could attempt to reduce its competitors' ability to compete by offering a strong Synopsys or Ansys product in one of the conglomerate leveraging markets, combined with one of the other Party's products at a bundled price lower than the sum of the standalone prices (mixed bundling). In the extreme, the Merged Entity could engage in pure bundling (also known as contractual tying) and refuse to sell the strong product on a standalone basis, but rather only as part of a bundle with the other Party's products. Both mixed and pure bundling could potentially lead to the anticompetitive marginalisation of rivals selling standalone products (i.e., non-integrated rivals) competing with the other Party's product and to consumer harm, if the bundled offer was not replicable and the bundling strategy diverted sufficient demand from non-integrated rivals to make them unable to compete effectively.

(541) However, the Commission notes that bundling as such is a common practice that often has no anticompetitive consequences, and that companies engage in bundling in order to provide their customers with better products or offerings in cost-effective ways.[497] Therefore, and in line with concerns raised by market participants, the Commission's assessment primarily focusses on technical tying via the total restriction or degradation of interoperability, and deals with anticompetitive bundling incidentally within each relevant sub-section.

5.4.4. The Notifying Party's view

(542) This Section proceeds by providing the Notifying Party's views that apply generally to all conglomerate relationships between EDA tools.

Ability

(543) The Notifying Party submits that the merged entity will lack the ability to foreclose competitors in the EDA markets by totally restricting or degrading interoperability or by means of anticompetitive bundling or tying.

(544) **First**, the Notifying Party considers that the merged entity would have no significant degree of market power in the supply of EDA products.[498] In particular, the Notifying Party submits that Cadence and Siemens are leading EDA providers with their own areas of considerable EDA strength, as well as extensive capabilities in multiphysics analysis tools.[499]

(545) **Second**, the Notifying Party submits that its rivals already can or would be able to offer alternative solutions or bundles integrating EDA tools.[500] Not only do Cadence and Siemens offer products in almost all the same segments as Synopsys; they also integrated multiphysics analysis solutions. By contrast, Synopsys presently relies on Ansys for multiphysics analysis capabilities.[501] Therefore, Cadence and Siemens could replicate any merged entity's solutions in a timely fashion through their own integrated solutions or by partnering with or acquiring

497 Non-Horizontal Merger Guidelines, para. 93.
498 Form CO, para. 1012 et seq.
499 Form CO, paras 1013.
500 Form CO, para. 1030.
501 Form CO, para. 1031.

other vendor's solutions.[502] These competitors could also retaliate by refusing future collaborations with their technology, for testing and support of new releases.[503]

(546) **Third**, the Notifying Party submits that the Merged Entity would have no ability to totally restrict or degrade interoperability to foreclose competitors.[504] In particular the Notifying Party notes that, customers insist on having the ability to customize their chip design flows with tools they consider "best of breed" based on the quality of results, performance and suitability to their particular needs.[505] An EDA that does not support industry standard formats would not be a credible alternative as it would not work with a customers' multi-vendor chip design workflow or be able to be read by foundries.

(547) **Fourth**, the Notifying Party submits that the Merged Entity would have no effective means to harm rivals by bundling or tying.[506]

(a) In the first place, customers would not be easily influenced by any leveraging strategy. EDA customers are highly sophisticated and insist on using the "best of breed" tools for their needs, and they would have the bargaining power to reject any tying attempts. Moreover, customers value the possibility of selecting the "best of breed" tools more than potential discounts on bundled tools.[507]

(b) In the second place, customers procure standalone tools as and when required rather than at a single point in time. Refusals to offer tools on a standalone basis would therefore dramatically reduce the sales opportunities for the merged entity.[508]

Incentive

(548) The Notifying Party submits that it would have no incentive to engage in any foreclosure strategy by totally restricting or degrading interoperability or by means of anticompetitive bundling or tying.[509]

(549) **First**, the Notifying Party submits that any foreclosure strategy would risk substantial financial losses.[510]

(a) In the first place, degrading interoperability would make the Merged Entity's products less attractive, if not unusable. In face of any foreclosure strategy, customers would switch to alternative suppliers or develop internally their chip design workflows so to be able to select "the best of breed" tools.[511]

(b) In the second place, any attempt at foreclosure strategy would significantly harm the Parties' reputation.[512]

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502 Form CO, para. 1048.
503 Form CO, paras 1098 et seq.
504 Form CO, para. 1049.
505 Form CO, para. 1050.
506 Form CO, para. 1090.
507 Form CO, paras 1091-1092.
508 Form CO, para. 1094.
509 Form CO, para. 1095.
510 Form CO, paras 1096-1097.
511 Form CO, paras 1096-1097.
512 Form CO, paras 1110-1111.

(550) **Second**, the Notifying Party submits that it has never attempted to degrade or restrict interoperability or to bundle products anticompetitively. Neither Ansys nor Synopsys has ever degraded the interoperability of its semiconductor-related tools and both Parties' EDA and S&A tools are also available on a standalone basis. [513]

Effects

(551) The Notifying Party submits that any foreclosure strategy would not significantly impede effective competition.[514]

(552) **First**, the Notifying Party submits that any foreclosure attempt would not materially affect competitors. Particularly, the Notifying Party's main rivals – Cadence and Siemens – can already match any offer from the Merged Entity post-Transaction using technologies from their broad portfolio of EDA solutions.[515]

(553) **Second**, the Notifying Party submits that EDA markets are dynamic and expanding, offering rivals many opportunities to compete. Rival EDA and S&A vendors are accelerating investments in innovation through internal R&D, acquisitions of key technologies, and strategical partnerships.[516]

(554) **Third**, the Notifying Party submits that the Transaction would have relevant procompetitive effects because it would enable more integrated versions of Synopsys and Ansys' tools. This would benefit customers who increasingly demand a more comprehensive solution for their analysis earlier in the chip design flow. Moreover, the Transaction would allow the merged entity to better compete with its integrated rivals, as Cadence and Siemens.[517]

5.4.5. Leveraging from Ansys' position in the market for gate-level power integrity analysis (RedHawk(-SC)) to foreclose Synopsys' rivals in the EDA markets

5.4.5.1. Potential concern

(555) Ansys is currently viewed as "Swiss-neutral" because it offers its EDA tools on a standalone basis and maintains effective interoperability with third-party EDA tools.[518] The concerns expressed by some market participants therefore primarily related to the Merged Entity's ability and incentive to change Ansys' "Swiss-neutral" approach to interoperability in order to foreclose competitors in the markets for EDA tools. The market participants expressing such concerns considered that the Merged Entity could leverage Ansys' potentially strong market position in the markets for several EDA tools such as power analysis, gate-level power integrity analysis and electromagnetic simulation but also more generally any other market for EDA tools where Ansys could potentially have market power, to achieve such result. However, the Commission notes that the foreclosure concerns raised by market participants focused primarily on the Merged Entity's ability and incentive to leverage Ansys' flagship product RedHawk(-SC) (a gate-level power integrity analysis tool) to foreclose competing providers of EDA tools. RedHawk(-SC) is considered the industry's "golden standard" and is viewed by

513 Form CO, paras 1113 et seq.
514 Form CO, para. 1120.
515 Form CO, para. 1121.
516 Form CO, paras 1122 et seq.
517 Form CO, para. 1133.
518 Market participant's response to the CMA's Questionnaire dated 21 October 2024, page 11.

many market participants as particularly important.[519] This fact is reflected in Ansys' revenues, where RedHawk(-SC) alone accounts for [a significant proportion] of Ansys' total EDA-related revenue.[520]

(556) Based on these elements, the Commission has assessed a potential competition concern whereby the Merged Entity would have the ability and incentive to leverage Ansys' potentially strong position in a global market for *gate-level power integrity analysis* where it has [50-60]% market share by revenue worldwide in 2023 with its tool RedHawk(-SC), into neighbouring EDA markets (based on both interoperability pairings and bundle pairings) where Synopsys is active[521], and whether such a foreclosure strategy would have a significant detrimental effect on competition in the relevant markets.

(557) The Commission has separately assessed two potential concerns relating to Ansys' gate-level power integrity tool RedHawk(-SC): (i) the total restriction or degradation of interoperability between Ansys' gate-level power integrity tool RedHawk(-SC) and third-party EDA tools and (ii) anticompetitive (pure and/or mixed bundling) with Ansys' gate-level power integrity tool RedHawk(-SC) and Synopsys' products.

5.4.5.1.1. Total restriction or degradation of interoperability (technical tying) between Ansys' gate-level power integrity analysis tool RedHawk(-SC) and third-party EDA tools

(558) A few market participants expressed concerns that the Merged Entity would have the ability and incentive to leverage Ansys' gate-level power integrity analysis tool RedHawk(-SC) to foreclose competing providers of EDA tools by totally restricting or degrading interoperability between Ansys and rival EDA tools.

(559) For instance, one market participant indicated that the Merged Entity has market power in gate-level power integrity, which it could leverage to foreclose competing EDA providers. According to the market participant, RedHawk(-SC) is "the industry gold-standard" for gate-level power integrity analysis,[522] and the Merged Entity would use its market power to totally restrict or degrade interoperability by (a) terminating the existing interoperability agreements and/or (b) impairing interoperability through code adjustments, ultimately achieving the same effect and/or (c) introducing new proprietary interfaces for the Merged Entity's tools.[523] In addition, the market participant considered that the Merged Entity would have an incentive to engage in a foreclosure strategy because customers would most likely switch to the combined entity's EDA tools that would continue to seamlessly interoperate, in contrast with competing EDA tools.[524]

(560) Another market participant was concerned that the Transaction will change Ansys' "Swiss-neutral" approach to interoperability between its EDA tools in general (including RedHawk(-SC)), and third parties' EDA tools.[525] According to the

519 See Section 5.4.5.3.1.1.
520 Form CO, para. 21.
521 See Annex A for an overview of the export-import relationships for gate-level power integrity analysis.
522 Market participant's response to the CMA's Questionnaire of 21 October 2024, question 13.
523 Market participant's submission to the CMA dated 12 April 2024, paras 2.13-2.14.
524 Market participant's submission to the CMA dated 12 April 2024, para. 2.15.
525 Market participant's submission to the European Commission dated 14 June 2024, paras. 118-119.

market participant, Ansys has consistently ensured that their tools can seamlessly interoperate with third-party tools while Synopsys has a documented history of degrading interoperability with its standalone tools. In the same vein, Synopsys will have the ability to delay, degrade or entirely restrict interoperability with the standalone versions of RedHawk(-SC) to drive customers towards its integrated solution. Since Synopsys is already integrating RedHawk(-SC) capabilities in some of its EDA tools today, it would require minimal effort for Synopsys to implement such a strategy.[526] Further, according to the market participant, Synopsys will also have the incentive to foreclose competitors, in particular in relation to tools that interoperate with Ansys' RedHawk(-SC) and that are critical for the chip design (e.g., timing and signal integrity analysis, place & route, electromagnetic interference).[527] In that respect, according to the market participant, in contrast with Ansys' track record, Synopsys' past practices confirm the clear incentive to delay, degrade, and even restrict interoperability.[528]

5.4.5.1.2. Anticompetitive (pure and/or mixed) bundling with Ansys' gate-level power integrity tool RedHawk(-SC) and Synopsys' products

(561) According to some market participants, the Merged Entity would have the ability to bundle Ansys' EDA tools, including RedHawk(-SC), and Synopsys' products.

(562) For instance, one participant stated that the Merged Entity will have market power in the supply of multiple design IP segments, as well as strong market positions in several complementary product categories including multiple EDA and CAE tools, and that it will have both the ability and incentive to bundle.[529]

(563) Another participant explained that the Merged Entity would have the ability to integrate Ansys' tools in its integrated offering and to engage in mixed bundling.[530]

5.4.5.2. The Notifying Party's view

(564) For the same reasons as outlined in Section 5.4.4 , the Notifying Party submits that the Merged Entity will lack the ability and the incentive to leverage Ansys' RedHawk(-SC) to foreclose competitors in the EDA markets by degrading/removing interoperability or by means of anticompetitive bundling/tying, and that any foreclosure strategy would not significantly impede effective competition.

(565) This Section also outlines specific views of the Notifying Party that apply to the Merged Entity's ability and incentive to leverage Ansys' potentially strong position in a global market for *gate-level power integrity analysis* (with its tool RedHawk(-SC)) and the effects of such foreclosure strategy.

Ability

(566) The Notifying Party submits that the Merged Entity would have no ability to foreclose Synopsys' rivals by leveraging RedHawk(-SC), particularly because Ansys has no market power with RedHawk(-SC) in gate-level power integrity

526 Market participant's response to the CMA's Questionnaire of 21 October, question 7.
527 Market participant's submission to the European Commission dated 14 June 2024, paras. 130-133.
528 Market participant's submission to the European Commission dated 14 June 2024, para. 133.
529 Market participant's submission to the CMA dated 12 April 2024, paras. 2.11-2.12.
530 Market participant's submission to the European Commission dated 14 June 2024, paras. 129.

analysis since Cadence's product Voltus is a strong competitor to RedHawk(-SC) and a highly popular solution among EDA customers[531] and Siemens' mPower is also an effective alternative to RedHawk(-SC).

Incentive

(567) The Notifying submits that the Merged Entity would have no incentive to leverage Redhawk to foreclose rivals in neighbouring markets that have interoperability relationships with RedHawk(-SC).[532]

(568) The Notifying Party submits that a strategy to leverage RedHawk(-SC) would not be commercially viable because, **first**, the customers could easily switch to the competing tools Voltus or mPower, removing the incentive[533]; **second**, Synopsys' industry-wide commitment to interoperability also applies to RedHawk(-SC) and degrading or removing interoperability between RedHawk(-SC) and competing tools would harm the reputation and credibility of RedHawk(-SC);[534] and, **third,** restricting interoperability would cripple RedHawk(-SC)'s ability to interoperate with tools from all vendors.

Effects

(569) The Notifying Party submits that such foreclosure strategy would have no appreciable effect on competition because, **first**, RedHawk(-SC) is not nearly as strong as core leveraging products in recent decisions where the Commission has raised conglomerate concerns[535]; and, **second**, RedHawk(-SC) will continue to face strong competition from both Voltus and mPower reducing any putative impact on effective competition.[536]

5.4.5.3. The Commission's assessment

5.4.5.3.1. Ability to foreclose

(570) For the reasons set out below, the Commission has reached the conclusion that the Merged Entity **would likely not have the ability** to engage in a strategy of market-wide foreclosure of its rivals in EDA markets whose tools interact with RedHawk(-SC) by totally restricting or degrading interoperability or engaging in anticompetitive (pure and/or mixed) bundling.

(571) **First**, the Commission cannot exclude that RedHawk(-SC) holds a significant degree of market power on the market for gate-level power integrity analysis (Section 5.4.5.3.1.1). **Second**, the Commission considers that the Merged Entity would likely not have the ability to foreclose competing providers of EDA tools by totally restricting or degrading interoperability between RedHawk(-SC) and third-party EDA tools (Section 5.4.5.3.1.2). **Third**, the Commission considers that the

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531 Parties' submission to the Commission, "Why Synopsys Could Not Leverage RedHawk to Harm Competitors", 29 August 2024, para. 8

532 Form CO, para. 21

533 Parties' submission to the Commission, "Why Synopsys Could Not Leverage RedHawk to Harm Competitors", 29 August 2024, para. 37

534 Parties' response to the Commission's RFI 14, para. 5.9

535 Parties' submission to the Commission, "Why Synopsys Could Not Leverage RedHawk to Harm Competitors", 29 August 2024, paras. 61-62

536 Parties' submission to the European Commission, "Why Synopsys Could Not Leverage RedHawk to Harm Competitors" dated 29 August 2024, para. 62

Merged Entity would likely not have the ability to foreclose competing providers of EDA tools by engaging in anti-competitive (pure and/or mixed) bundling between RedHawk(-SC) and Synopsys' EDA tools (Section 5.4.5.3.1.3)

5.4.5.3.1.1. Assessment of Ansys' potential market power in the worldwide market for gate-level power integrity analysis

(572) For the reasons explained below, **the Commission cannot exclude that Ansys holds a significant degree of market power in the worldwide market for gate-level power integrity analysis**. This is because, whilst the market investigation showed that there are some relevant alternatives to RedHawk(-SC), itremains the leading product on the market that is singled out for its strength and quality.

(573) **First**, the Commission notes that Ansys holds a significant market share in gate-level power integrity (in digital chip design) with RedHawk(-SC)*:* [50-60]% worldwide by revenue in 2023. The only other providers of gate-level power integrity tools are Cadence (Voltus; [30-40]% worldwide by revenue in 2023) and Siemens (mPower; [5-10]% worldwide by revenue in 2023).

(574) **Second**, RedHawk(-SC) is widely considered by market participants as a "golden standard" / "best-in-class" tool in its category. For instance, one market participant explains that "*Ansys Redhawk-SC is a leading industry tool for power integrity and reliability signoff*"[537]. Another market participant explains that "*Redhawk-SC is unique as it is considered as the 'best in class' tool for Sign Off. It has better performance and overall quality compared to other tools*."[538]

(575) **Third**, Ansys' strong position in gate-level power integrity analysis is also reflected in the internal documents of Synopsys and Ansys.[539]

(576) **Fourth**, there are only two alternatives to Ansys' RedHawk(-SC) tool, Cadence's Voltus and Siemens' mPower, and both are widely considered weaker compared to RedHawk(-SC).[540]

(577) **With regard to Voltus**, the market investigation shows that many market participants consider Redhawk(-SC) to be superior, as it *inter alia* appears from the total average rating given to Voltus (3.5/5) compared to Redhawk(-SC) (4.5/5) when asked to rate the strength/quality of the tool.[541] Furthermore, the results of the Commission's market investigation suggest that Voltus does not have the same status as Redhawk(-SC) in terms of "market trust". According to one of the respondents to the Commission's market investigation, "*Cadence's Voltus IC can be considered an alternative tool to Ansys' RedHawk(-SC). The basic functions of Voltus IC are the same as RedHawk, but there is a lack of data for consistency in all functions, so the market trust has not reached that of RedHawk*".[542]

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537 Reply to Questionnaire to customers of EDA and Design IP, question D.A.C.3.

538 Reply to Questionnaire to customers of EDA and Design IP, question D.A.C.3

539 See for example Synopsys internal document, Annex PN RFI 4 – Q.13.3.pdf ; Synopsys internal document, Annex PN RFI 4 – Q.15, ", […]; Ansys internal documents, Annex PN RFI 4 – Q.13.3, […].

540 Reply to Questionnaire to customers of EDA and Design IP, question D.A.C.2

541 Reply to Questionnaire to customers of EDA and Design IP, question D.A.C 2

542 Reply to Questionnaire to customers of EDA and Design IP, question D.A.C 3

(578) **With regard to mPower**, the market investigation also shows that many market participants consider that Redhawk(-SC) is superior, as it *inter alia* appears from the total average rating given to mPower (3.13/5) compared to Redhawk(-SC) (4.5/5) when asked to rate the strength/quality of the tool.[543] Further, the preliminary market investigation shows that mPower is not yet adopted by significant customers. For instance, a market participant contacted during the preliminary market investigation explains that "*Siemens' mPower solution is still in a development phase and offers fewer features than existing solutions.".*[544]

(579) **Fifth**, the barriers to enter the gate-level power integrity analysis market are high. The majority of the market participants considered that it is unlikely that a new provider could launch a competitive gate-level power integrity analysis tool within the next two years.[545] One market participant to the Commission's market investigation replied that "*There are already other choices for gate level power integrity analysis from Cadence and Siemens. It would be easier for these suppliers to address shortfalls or gaps in their existing tools, than it would be for a new provider to launch a more competitive power consumption analysis product portfolio*."[546] Regarding the timeframe of two years, one market participant mentions in its response that "*It would take longer than two years to develop a competing technology*."[547]. Another market participant explains that "*Generally 2 to 3 years after merge of EDA companies, a new product or integration tend to happen.*"[548]. Furthermore, several market participants noted that about a decade ago Synopsys tried to enter by developing a competing Power Integrity tool (*PrimeRail*) but did not achieve sufficient quality. In 2017, it entered into a partnership with Ansys instead.[549]

(580) **Sixth**, it is expensive and time-consuming to switch to another gate-level power integrity tool, making it difficult for customers to stop using RedHawk(-SC) in favour of a competing tool. For instance, market participants that replied to the Commission's market investigation mentioned that "*Switching EDA vendors is very expensive and time-consuming*" and that it can take "*3-years EDA contract + training of engineers + change only when starting a new project ... so better to remain with a tool if it is answering the needs.*"[550] Finally, a market participant explains that "*Redhawk has been in the market for a [confidential] period, making it difficult for customers to switch away, as engineers develop a preference for the tools they are accustomed to, leading to a certain "stickiness" with these products. Engineers also script functionality and routines around their incumbent tools, making them even more challenging for competitive displacement*."[551]

(581) On the basis of all these elements, and for the purposes of this Decision, the Commission cannot exclude that Ansys has a significant degree of market power in

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543 Reply to Questionnaire to customers of EDA and Design IP, question D.A.C.2

544 Market participant's submission to the European Commission dated 14 June 2024, para. 86.

545 Reply to Questionnaire to customers of EDA and Design IP, question D.A.C.4.2

546 Reply to Questionnaire to customers of EDA and Design IP, question D.A.C.4.3

547 Reply to Questionnaire to customers of EDA and Design IP, question D.A.C.4.3

548 Reply to Questionnaire to customers of EDA and Design IP, question D.A.C.4.3

549 Reply to Questionnaire to customers of EDA and Design IP, question D.A.C.4.3. See also Market participant's submission to the European Commission dated 14 June 2024, para. 7414. and Minutes of a call with a market participant dated 23 July 2024, para. 7.

550 Reply to Questionnaire to customers of EDA and Design IP, question D.A.6

551 Minutes of a call with a market participant dated 27 June 2024, para. 11.

the worldwide market for gate-level power integrity analysis with its RedHawk(-SC) tool.

5.4.5.3.1.2. The Merged Entity's ability to foreclose competing providers of EDA tools by totally restricting or degrading interoperability between RedHawk(-SC) and third-party EDA tools

(582) For the reasons explained below, the Commission considers it **unlikely that the Merged Entity would have the ability** to engage in a strategy of market-wide foreclosure of competing providers of EDA tools by totally restricting or degrading interoperability between RedHawk(-SC) and third-party EDA tools in any of the affected interoperability pairings relating to Ansys' tools in gate-level power integrity specified in Annex A of the Decision.

(583) **First**, the Commission cannot exclude that the Merged Entity could have the ability to *degrade* interoperability between RedHawk(-SC) and third-party EDA tools based on proprietary interfaces. However, the Merged Entity would likely not have the technical ability to *totally restrict* interoperability between RedHawk(-SC) and third-party EDA tools, because effective interoperability will remain possible based on industry-standard interfaces for almost all affected interoperability pairings, or customers could potentially find workaround solutions to continue using the given EDA tools (Sections 5.4.5.3.1.2.1 and 5.4.5.3.1.2.2). **Second**, even if it was possible to technically totally restrict or degrade interoperability, the Merged Entity would unlikely engage in this foreclosure mechanism to foreclose its EDA rivals (Section 5.4.5.3.1.2.3). **Third**, even if the Merged Entity totally restricted or degraded interoperability between RedHawk(-SC) and third-party EDA tools, the Commission considers that the Merged Entity would not have the ability to leverage Ansys' position in the market for gate-level power integrity analysis with RedHawk(-SC), because it is unlikely that a significant proportion of customers would switch to EDA tools of the Merged Entity as a result of foreclosure of third-party EDA tools (Section 5.4.5.3.1.2.4). **Fourth**, even if the Merged Entity would have the ability to leverage its position in the market for gate-level power integrity, the Commission considers that Synopsys' main rivals in the EDA markets, Cadence and Siemens, would be able to deploy effective and timely counterstrategies in the face of any foreclosure strategy (Section 5.4.5.3.1.2.5).

5.4.5.3.1.2.1. Technical ability to hamper interoperability between RedHawk(-SC) and third-party EDA tools

(584) As outlined in Sections 3.5 and 5.4.3.1, interoperability between RedHawk(-SC) and third-party EDA tools is achieved through baseline interoperability and/or proprietary interfaces.

(585) As Table 44 below shows, the interoperability between RedHawk(-SC) and third-party EDA tools is currently predominantly based on industry-standard file formats. In 11 out of 12 affected interoperability pairings involving RedHawk(-SC) as a gate-level power integrity analysis tool, RedHawk(-SC) imports from or exports to third-party EDA tools based only on industry-standard file formats.

(586) There is therefore only **1** affected conglomerate link involving RedHawk(-SC) as a gate-level power integrity analysis tool, where interoperability between RedHawk(-SC) and third-party EDA tools is (also) based on proprietary interfaces. This is the

case between RedHawk(-SC) and Cadence's timing analysis tool Tempus and only when RedHawk(-SC) is importing from Tempus.[552] When Cadence's Tempus exports data to RedHawk(-SC), Ansys requests that it does so in a file format that is defined by Ansys. No other proprietary connections exist today between Synopsys' rivals' timing analysis tools and RedHawk(-SC).[553] Further, Ansys currently does not have nor was planning to develop any additional proprietary connections between RedHawk(-SC) and third-party (non-Synopsys) EDA tools in 11 of those EDA tools pairings. The Commission also understands that no customer or third-party EDA provider made such a request to Ansys. [554]

Table 44: Interoperability between Ansys' gate-level power integrity analysis tool RedHawk(-SC) and third-party (non-Synopsys) EDA tools

Data flow direction	Function of third-party (non-Synopsys) EDA tools that interoperate with Ansys' gate-level power integrity tool (RedHawk(-SC))	Interoperability format
RedHawk(-SC) […]	Place & route	Industry standards
RedHawk(-SC) […]	Simulation verification	Industry standards
RedHawk(-SC) […]	Layout	Industry standards
RedHawk(-SC) […]	Parasitic extraction	Industry standards
RedHawk(-SC) […]	Characterisation	Industry standards
RedHawk(-SC) […]	ECO	Industry standards
RedHawk(-SC) […]	Gate-level power consumption analysis	Industry standards
RedHawk(-SC) […]	Design robustness	Industry standards
RedHawk(-SC) […]	Emulation-based power analysis	Industry standards
RedHawk(-SC) […]	RTL power consumption analysis tools	Industry standards
RedHawk(-SC) […]	Functional safety & specification analysis	Industry standards
RedHawk(-SC) […]	Timing analysis	Industry standards […].[…]

552 When RedHawk(-SC) exports to third-party timing analysis tools, it does so in an industry-standard file format.

553 Ansys requests Cadence's Tempus as well as Synopsys' PrimeTime to write the text file in a format that can be read by RedHawk(-SC) (this can be referred to as the RedHawk file format or Timing Data Files).

554 Parties' response to the European Commission's RFI 22, paras 12.1 and 12.2.

(587) The Commission has considered the differences between two types of interoperability in assessing the Merged Entity's technical ability to totally restrict or degrade interoperability, and investigated whether the Merged Entity could (i) totally restrict or degrade interoperability between RedHawk(-SC) and third-party EDA tools currently based on proprietary interfaces, and separately whether it could (ii) totally restrict or degrade interoperability between RedHawk(-SC) and third-party EDA tools based on industry-standard interfaces.[555]

(588) The following sections discuss separately the Merged Entity's technical ability to totally restrict or degrade (a) interoperability based on proprietary interfaces and (b) interoperability based on industry standards.

a. Technical ability to hamper interoperability between RedHawk(-SC) and third-party EDA tools based on proprietary interfaces

(589) **As regards the Merged Entity's technical ability to totally restrict or degrade interoperability between RedHawk(-SC) and third-party timing analysis tools based on proprietary interfaces (i.e. Cadence's Tempus tool)**, the Commission considers that the Merged Entity would unlikely have the ability to totally restrict such interoperability but cannot exclude its ability to *degrade* such interoperability, for the following reasons.

(590) **First**, the majority of customers providing a view in the market investigation, consider that it would be unlikely or even impossible for the Merged Entity to *totally remove* interoperability based on proprietary interfaces between RedHawk(-SC) and EDA tools from a competing EDA vendor.[556] Further, the majority of competitors participating in the market investigation also did not consider that the Merged Entity would have such an ability.[557]

(591) **Second**, the customers submitting their views in the market investigation provided mixed opinions on whether the Merged Entity would have the ability to *degrade* interoperability between RedHawk(-SC) and third-party EDA tools based on proprietary interfaces.[558] The majority of competitors participating in the market investigation did not consider that the Merged Entity would have such an ability.[559]

(592) The market participants indicated several ways in which the Merged Entity could degrade interoperability between RedHawk(-SC) and third-party timing analysis tools. Firstly, according to one market participant, the Merged Entity could develop proprietary interfaces that are only optimised for their tools. Secondly, the Merged Entity could strategically prioritize its own EDA tools by developing new features and capabilities and enhancing interoperability between its own EDA tools, while deprioritizing interoperability with rival EDA vendors.[560] Thirdly, the Merged Entity could make Ansys' RedHawk(-SC) import and export data in proprietary formats that cannot be read by third-party EDA tools.[561] [562]

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555 The technical ability to engage in bundling is not assessed since it is theoretically possible to bundle many EDA tools, because many EDA tools in the chip design flow, as well as design IP, are interrelated and complementary in nature, and thereby could potentially be sold together in a bundle.

556 Replies to Questionnaire to customers of EDA and design IP, question D.B.A.8.

557 Replies to Questionnaire to competitors in EDA and design IP, question D.B.A.4.

558 Replies to Questionnaire to customers of EDA and design IP, question D.B.A.8.

559 Replies to Questionnaire to competitors in EDA and design IP, question D.B.A.4.

560 Replies to Questionnaire to customers of EDA and design IP, question D.B.A.9.1.

561 Replies to Questionnaire to customers of EDA and design IP, question D.B.A.9.1.

(593) **Third**, despite different mechanisms to degrade interoperability based on proprietary interfaces described by some market participants, the Commission notes that the Merged Entity would have a limited scope to degrade interoperability between RedHawk(-SC) and rival timing analysis tools.

(594) In the first place, [details of Ansys' interoperability agreements with competitors]. Cadence's timing analysis tool exports data to RedHawk(-SC) in a non-proprietary text file and does not depend on Ansys' tool to perform its function. Degrading interoperability between RedHawk(-SC) and Cadence's timing analysis tool Tempus would require the Merged Entity to alter the format that has already been defined by Ansys, and which today enables RedHawk(-SC) to import data from Cadence's timing analysis tool based on which it performs voltage drop analysis.

(595) In the second place, Ansys' RedHawk(-SC) does not presently have a proprietary connection with timing analysis tools of other Merged Entity's rivals such as Siemens, which the Merged Entity could degrade.

(596) In the third place, the Commission considers that the Merged Entity would have a limited scope to make Ansys' RedHawk(-SC) import and export data only in proprietary file formats (for instance, in a proprietary FSDB file format that is owned by Synopsys), such that RedHawk(-SC) cannot interoperate with third-party EDA tools based on industry-standard interfaces. The Commission understands that only five Ansys tools write FSDB, including RedHawk(-SC), and that Ansys' tools write FSDB primarily for [details of the coverage of Ansys' interoperability agreements]. In other words, there are no affected interoperability pairings involving Ansys' tool writing FSDB as an input for Synopsys' rivals EDA tools. In addition, FSDB is not an overarching file format that can serve all EDA functions.[563] By making Ansys' RedHawk(-SC) read and write in FSDB file format only, the Merged Entity would render RedHawk(-SC) unusable with most of EDA tools for which FSDB is not the appropriate file format.[564]

(597) **Fourth**, the EDA tools' customers may find workaround solutions to solve and prevent interoperability issues. Based on the results of the market investigation, several customers submitted that they would find a workaround solution to solve or avoid any interoperability issues. The Parties' internal documents reflect several instances where customers have maintained effective interoperability by building their workarounds. In one such instance Synopsys' customer [customer name] manually edited data exported by Cadence's tools [tool name] such that it could be imported in Synopsys' EDA tools [tool name]. In another example, Synopsys' customer [customer name] devised a workaround solution by converting an industry-standard file format (VCD) into a proprietary format that can be read by Synopsys' tool Verdi (FSDB). Similarly, another customer of Synopsys, [customer name], manually converted an output written in a proprietary file format into an industry standard file format (VCD) to enable the interoperability link between third-party EDA tools.[565]. [566]

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562 Market participant's submission to the CMA dated 12 April 2024, question 7.
563 Parties' response to the Europan Commission's RFI 25, paras 22.1-22.5.
564 Parties' response to the Europan Commission's RFI 25, paras 22.1-22.5.
565 Replies to Questionnaire to customers of EDA and design IP, question D.B.A.12.
566 Parties' response to the European Commission's RFI 26, para. 7.1-7.3.

(598) Based on the elements considered above, and for the purposes of this Decision, the Commission concludes that the Merged Entity would unlikely have the ability to *totally restrict* interoperability between RedHawk(-SC) and third-party EDA tools based on proprietary interfaces, but cannot exclude its ability to *degrade* such interoperability However, even if the Merged Entity would have the technical ability to degrade interoperability based on proprietary interfaces, for the reasons explained in more detail in Section 5.4.5.3.1.2.2, the Commission considers that third-party EDA tools could still effectively interoperate with Ansys EDA tools (including RedHawk(-SC)) based on industry standards, which is the case for almost all interoperability pairings involving RedHawk(-SC). In any event, for the reasons explained in more detail in Section 5.4.5.3.1.2.3 below, the Commission considers it unlikely that the Merged Entity would engage in this foreclosure mechanism. This is also strongly in line with the feedback the Commission received in the market investigation. Namely, while some customers submitted that it would be "possible" to degrade interoperability based on proprietary interfaces, several of such customers added that they do not consider it likely.

b. Technical ability to hamper interoperability between RedHawk(-SC) and third-party EDA tools based on industry standards

(599) **As regards the Merged Entity's technical ability to restrict or degrade interoperability between RedHawk(-SC) and third-party EDA tools ensured through industry-standard file formats (i.e., baseline interoperability)** the Commission considers that the Merged Entity would likely not have such an ability, for the following reasons.

(600) **First**, the Commission's market investigation confirms that the Merged Entity would unlikely have the ability to totally restrict or degrade baseline interoperability between RedHawk(-SC) and third-party EDA tools.

(601) In the first place, the Commission notes that EDA suppliers have a very limited scope to hamper interoperability based on industry-standard file formats due to the very process of their implementation. EDA vendors perform unilateral checks to verify whether their EDA tools correctly implement industry-standard file formats, which is primarily done without any interoperability agreements between EDA vendors. To validate their tools' compatibility with industry-standard file formats, EDA vendors rely on the specifications and manuals published by the standards committee or industry consortium that maintains the standard in question. Therefore, unilateral checks do not require any third-party documentation or know-how or access to rivals' EDA tools or documentation, and the EDA vendor's implementation of industry-standard file formats is not dependent on the action of rival EDA vendors (including the Merged Entity). Once the unilateral checks are done, the EDA tool is presumed to work with all third-party tools that implement the same industry-standard file format. Should the Merged Entity want to terminate or degrade baseline interoperability, it would have to hamper its own unilateral checks, which in practice would mean declining to confirm that its own EDA tools conform to industry standards.[567] [568]

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567 Parties' Paper on the Baseline Interoperability in EDA, paras. 19-25.

568 As explained in Section 5.4.3.1.1, baseline interoperability may be supplemented by interoperability agreements between EDA vendors for the purpose of testing and bug-fixing ("debugging agreements"). The Commission has therefore also considered whether the Merged Entity would have the ability to restrict or degrade baseline interoperability by failing to fulfil their obligations from any

(602) In the second place, the majority of market participants providing a view in the market investigation also confirmed that it is unlikely or even impossible that the Merged Entity would totally *remove* baseline interoperability between RedHawk(-SC) and third-party EDA tools.[569] Similarly, the majority of market participants providing a view in the market investigation considered that the Merged Entity would unlikely have the ability to *degrade* such interoperability.[570]

(603) **Second**, the Commission has also considered past behaviour of Synopsys and Ansys with respect to interoperability with their rivals' EDA tools, and found no indications of the Parties totally restricting or degrading baseline interoperability. In that regard, the majority of customers providing their views submitted that Synopsys, Ansys, Cadence, Siemens or other EDA vendors never terminated/denied, degraded the quality and/or delayed interoperability between their own EDA tools and EDA tools of another vendor.[571] The same experience was confirmed by the majority of competitors providing their views in the market investigation.[572]

(604) **Third**, the Commission has not found any evidence in the Parties' internal documents indicating that restricting or degrading interoperability based on industry-standard file formats with rival EDA tools was attempted in the past or planned in the future.

(605) **Fourth**, as explained in Section 5.4.5.3.1.2.1 a) above, the results of the market investigation and the Parties' internal documents indicate that customers may find workaround solutions to solve and prevent interoperability issues.

(606) Based on the elements considered above, and for the purposes of this Decision, the Commission has reached the conclusion that the Merged Entity would likely not have the technical ability *to totally restrict or degrade* interoperability between RedHawk(-SC) and third-party EDA tools based on industry standards.

5.4.5.3.1.2.2. No technical ability to hamper interoperability between RedHawk(-SC) and third-party EDA tools because industry standards will remain to ensure effective interoperability between EDA tools

(607) Based on the elements considered in Sections 5.4.5.3.1.2.1 a) and b) above, and for the purposes of this Decision, the Commission considers that even if the Merged Entity would have the technical ability to degrade interoperability based on *proprietary interfaces*, the Merged Entity would likely **not have the technical ability to totally restrict interoperability** between RedHawk(-SC) and third-party EDA tools, because (i) effective interoperability will remain possible based on industry-standard interfaces for almost all affected interoperability pairings

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such agreements. However, the results of the market investigation have shown that, while debugging agreements may facilitate interoperability, industry-based standard interfaces sufficiently guarantee effective interoperability. Replies to Questionnaire to competitors in EDA and design IP, questions D.B.A.3.

569 Replies to Questionnaire to customers of EDA and design IP, question D.B.A.4.

570 Replies to Questionnaire to customers of EDA and design IP, question D.B.A.8.

571 Replies to Questionnaire to customers of EDA and design IP, question C.B.3.

572 Replies to Questionnaire to competitors in EDA and design IP, question C.B.1.

involving RedHawk(-SC), and (ii) customers can and do find workaround solutions to solve and prevent interoperability issues.[573]

(608) **First**, as explained in Section Section 5.4.5.3.1.2.1 above, interoperability between Ansys' RedHawk(-SC) and third-party EDA tools is predominantly based on industry-standard file formats, which the Merged Entity would unlikely have the technical ability to totally restrict or degrade.

(609) **Second**, in only 1 interoperability pairing where RedHawk(-SC) interoperates with third-party EDA tool based on proprietary interfaces, ([details of Ansys' interoperability agreements]), there is no industry-standard file format that can serve as an alternative to the proprietary interfaces. However, the Commission notes that even in exceptional instances where there is no industry-standard alternative that allows for interoperability between respective EDA tools (such as is the case for the affected interoperability pairing between RedHawk(-SC) and Cadence's timing analysis tool Tempus), the EDA tools' customers may find workaround solutions to solve and prevent interoperability issues.Based on the elements considered above, and for the purposes of this Decision, the Commission cannot exclude that the Merged Entity could have the ability to *degrade* interoperability between RedHawk(-SC) and third-party EDA tools (by degrading proprietary interfaces). However, the Merged Entity would likely not have the technical ability to *totally restrict* such interoperability.

5.4.5.3.1.2.3. Total restriction and/or degradation of interoperability is an unlikely foreclosure strategy because interoperability is an important element of the EDA industry

(610) For the reasons explained below, the Commission considers that even if it would be technically possible to degrade interoperability (by degrading proprietary interfaces, as discussed above), the Merged Entity would unlikely engage in this foreclosure mechanism to foreclose its EDA rivals.

(611) **First**, interoperability is an important element of the EDA industry. Due to the characteristic features of demand and supply in the EDA industry described in Section 5.4.3.1.2 , EDA vendors are generally incentivised to maintain effective interoperability in the EDA markets.

(612) In that regard, the Commission notes that Synopsys and [competitor] recently completed the annual renewal of their interoperability agreements. Similarly, Synopsys and [competitor] recently concluded the annual renewal of Interoperability Cross-License Agreement, their contractual framework for all of their interoperability agreements. Further, Synopsys and [competitor] recently agreed on [Details of Synopsys' renewals of its interoperability agreements with other EDA vendors].[574].[575] .[576]

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573 Of the seven affected conglomerate links between Ansys' EDA tools and third-party EDA tools that involve interoperability based on proprietary interfaces, there are alternative industry standard file format in five cases. Only two of these seven pairings do not have an industry-standard file format alternative.

574 Parties' response to the European Commission's RFI 25, para. 27.2.

575 Parties' e-mail to the European Commission, '[…]', and the attached adopted […].

576 The Commission understands that [information on Synopsys' interoperability agreement with an EDA vendor].

(613) **Second**, interoperability is particularly important for EDA tools used in the "sign-off" stage at the end of the chips design process, such as RedHawk(-SC), whose primary task is to read the data outputted by EDA tools used earlier in the chip design flow.

(614) In the first place, the Commission notes that interoperability appears necessary for the sign-off tools to reliably execute their functionality. Because of the extent to which customers mix-and-match EDA tools across the chip design process, interoperability between EDA tools is important. This principle applies most strongly to sign-off tools such as RedHawk(-SC), which mainly import (rather than export) data from other EDA tools. The purpose of sign-off tools is to read the output of design and implementation EDA tools and verify whether the planned chip design can be successfully manufactured by a foundry.[577] Therefore, they must be able to read the output of preceding EDA tools to do such verification.

(615) In the second place, since they mainly read the output of preceding EDA tools from different EDA vendors, sign-off tools such as RedHawk(-SC) need to remain "neutral" such that they can read different file formats. Namely, different EDA tools output in different file formats, which depend on the data exchanged between given EDA tools and the type of analysis done by the EDA tools. In consequence, there is no single overarching file format (whether industry-based or proprietary) based on which a sign-off tool could universally read the output of all preceding EDA tools. Limiting a sign-off tool's ability to read certain file formats would in practice mean that the given sign-off tool could read the output of some but not all EDA tools, and only sign off on a part of the chip.[578] This "neutrality" requirement applies to all sign-off tools. Indeed, EDA vendors prominently market their sign-off tools as supporting industry standard formats and being compatible with different solutions. For example, Siemens advertises its gate-level power integrity tool mPower as able to work with '*any design, any technology*' and reads '*industry standard inputs'*.[579] Cadence markets its gate-level power integrity tool Voltus as including '*support for all industry-standard vector formats*'.[580] Likewise, Synopsys advertises its timing analysis tool PrimeTime as offering '*extensive support for industry-standard input and output file formats'*.[581]

(616) In the third place, the Commission notes that in some instances RedHawk(-SC) interoperates with several different EDA tool functionalities based on the same industry-standard file format. For example, RedHawk(-SC) can read and write LEF/DEF (a type of industry standards) to interchange with third-party place & route tools. However, the same industry standard LEF/DEF is also supported by RedHawk(-SC) to interchange with architectural design & implementation tools and ECO tools. Totally restricting or degrading the support for industry standards may therefore have significant repercussions in practice. Hampering RedHawk(-SC)'s support for LEF/DEF in the example above would impact not only

577 For instance, Parties' Paper on the Lack of Interoperability Concerns, para. 55.

578 Parties' response to the European Commission's RFI 14, paras 5.16-5.19.

579 Siemens website, "mPower power integrity analysis", https://eda.sw.siemens.com/en-US/ic/mpower/, (last accessed on 8 January 2025).

580 Cadence website, "Voltus IC Power Integrity Solution" https://www.cadence.com/en_US/home/tools/digital-design-and-signoff/silicon-signoff/voltus-ic-power-integrity-solution.html#power, (last accessed on 8 January 2025).

581 Synopsys datasheet, "Golden Timing Signoff Solution and Environment", https://www.synopsys.com/content/dam/synopsys/implementation&signoff/datasheets/primetime-ds.pdf, (last accessed on 8 January 2025).

RedHawk(-SC)'s interoperability pairing with place & route tools, but any other EDA tools that interchange with RedHawk(-SC) on this basis.

(617) **Third**, as described in Section 5.4.3.1.2 customers have a significant role in demanding and maintaining effective interoperability, which the Commission considers significantly limits the Merged Entity's ability to totally restrict or degrade interoperability at its own initiative.

(618) The finding that the Merged Entity would unlikely engage in total restriction and/or degradation of interoperability is also strongly in line with the feedback the Commission received in the market investigation. Namely, while some customers submitted that it would be "possible" to totally restrict or degrade interoperability, several of such customers added that they do not consider it likely. As one customer observed, even if some measures to reduce interoperability might be technically feasible, "*the broader implications for user experience, competitive positioning, and industry standards make it unlikely that total removal would be practical or beneficial in the long run*."[582] Other customer observed that "*it feels unlikely that this would make commercial sense from the investment into locking the tool and the reduction in [the] market from lack o[f] interoperability*", that "*it should be possible but commercially not due to resistance from customers*", and that "*(a)ll of these are possible, but not likely (…). It would be a roadmap to go out of business"*.[583]

(619) Therefore, based on the elements considered above, and for the purposes of this Decision, the Commission considers that even it would be technically possible to degrade interoperability (by degrading proprietary interfaces), the Merged Entity would unlikely engage in this foreclosure mechanism.

5.4.5.3.1.2.4. Not a significant proportion of customers would switch to the Merged Entity's EDA tools as a result of foreclosure

(620) For the reasons explained below, the Commission considers that, even if the Merged Entity totally restricted or degraded interoperability between RedHawk(-SC) and third-party EDA tools, the Merged Entity would not have the ability to leverage Ansys' position in the market for gate-level power integrity with RedHawk(-SC) to foreclose Synopsys' rivals in the EDA markets. This is because it is unlikely that a significant proportion of customers would switch to EDA tools of the Merged Entity as a result of foreclosure. As a result, even if the Merged Entity could fully leverage its alleged market power with RedHawk(-SC), the Merged Entity would likely still not be able to foreclose Synopsys' rivals in the EDA markets.

(621) **First**, the market investigation indicates that customers would likely not switch their EDA tool at the benefit of the Merged Entity, as a result of foreclosure.

(622) In the first place, a majority of customers that expressed a view indicated that, in response to a hypothetical scenario where Ansys' RedHawk(-SC) is no longer interoperable with competitors' (non-Synopsys) EDA tools, they would switch to an alternative of RedHawk(-SC) (rather than switch to a Synopsys EDA tool that

582 Replies to Questionnaire to customers of EDA and design IP, question D.B.A.8.1.
583 Replies to Questionnaire to customers of EDA and design IP, question D.B.A.5.

continues to interoperate with RedHawk(-SC)).[584] This is true for all EDA tools that are interoperable with RedHawk(-SC).[585] In addition, a majority of customers that expressed a view indicated they would do the same even when confronted with a degradation or delay of interoperability (as opposed to a removal of interoperability).[586] For instance, one customer explained that it "*if we had issues with support for other point tools, we would consider an alternative gate level power integrity tool [and] most likely switch to […] Voltus*."[587] In that regard, one customer explained that it "*would have the opportunity and capacity to switch to alternatives, in case the Parties (or any other EDA vendors) would bundle, tie or integrate their tools, in such a way to make them less interoperable with other vendors' tools*."[588] Another market participant stated that "*EDA customers possess sufficient bargaining power to ensure this interoperability, mainly because customers tend to have a multi-sourcing strategy for their EDA tools, which ensures they always have alternatives to any specific EDA vendor's tools, and therefore the ability to switch to competitors if an EDA vendor degrades the interoperability of its products.*"[589]

(623) In the second place, *the Commission notes several of examples of customers that recently switched away from Ansys' RedHawk(-SC) to competing EDA tools.* [Examples of instances where Ansys' customers switched to alternative tools].[590].[591].

(624) **Second**, some customers already multi-home for their EDA tools (i.e. use two EDA vendors for one type of tool), including RedHawk(-SC). This enables customers to circumvent the foreclosure strategies of the Merged Entity, because they already have alternatives in place and can more easily switch from RedHawk(-SC).

(625) In the first place, the market investigation confirmed that customers multi-home their EDA tools in general. A majority of customers indicated that they use or plan to use two or more EDA vendors for the same EDA tool functionality.[592] Customers generally submitted that although there were costs to such a strategy, the benefits outweighed these costs.[593] For instance, the customers mentioned several advantages to having two alternative EDA suppliers for the same EDA tool functionality such as ensuring "*closer vendor competition*", "*vendor flexibility and negotiation*", "*access [to] the best in class tool*" and "*risk mitigation*".[594] Another customer mentioned that "*having at least two tools for the same job increases our confidence that the result are accurate*".[595] Finally, a customer explained that

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584 Replies to Questionnaire to customers of EDA and design IP, question D.B.A.10.

585 Place & route, simulation verification, layout, timing analysis, parasitic extraction, characterization, ECO, gate-level power consumption analysis, design robustness, emulation-based power analysis, RTL power consumption analysis, and functional safety and specification analysis.

586 Replies to Questionnaire to customers of EDA and design IP, question D.B.A.12.

587 Replies to Questionnaire to customers of EDA and design IP, question D.B.A.11 and D.B.A.13.

588 Minutes of a call with a market participant dated 24 June 2024, para. 19.

589 Minutes of a call with a market participant dated 24 June 2024, para. 18.

590 Parties' response to the European Commission's RFI 14, para. 10.1; Parties' response to CMA Issues Letter, para. 7.12.

591 The so-called "hierarchical analysis" is an advanced technique for analysing large chip designs more quickly.

592 Replies to Questionnaire to customers of EDA and design IP, question C.A.7.

593 Replies to Questionnaire to customers of EDA and design IP, question C.A.7.1.

594 Replies to Questionnaire to customers of EDA and design IP, question C.A.7.1.

595 Replies to Questionnaire to customers of EDA and design IP, question C.A.7.1.

"*having multiple tool flows can create competition for EDA companies to increase their investment to improve tool performance and quality*."[596]

(626) In the second place, customers multi-home primarily to ensure they always have the highest quality EDA tool for a given project, and to increase their bargaining power vis-à-vis EDA vendors. For instance, one customer explained that "*[its] strategy is to generally source EDA tools from two or occasionally three suppliers in order to pick the technically best tool for each design step.*"[597] Another customer stated that "*[the customer] tries to have a two-supplier strategy, in order to increase its bargaining power with EDA and S&A vendors.*"[598] A third customer stated it "*works with all EDA companies. Unlike other customers of EDA tools, [the customer] purchases contracts and licenses that give access to the entire portfolio of EDA companies' products. [The customer] chooses to procure EDA tools in this way so that [the customer] does not limit itself to a specific set of tools or companies. This extended access gives [the customer] possibility to pick and choose, as well as switch between tools in a short period between 2-6 months.*"[599]

(627) In the third place, the market investigation confirmed that some customers multi-home also with respect to their gate-level power integrity tool. Around 18% of customers using gate-level power integrity tool indicated that they have been using Ansys' RedHawk(-SC) as well as a gate-level power integrity tool of another vendor (Voltus, mPower or other).[600] In addition, to the best of its knowledge, Ansys submitted that at least [a significant percentage] % of its top 20 RedHawk(-SC) customers in 2023 also use [tool name] as an alternative gate-level power integrity tool.[601]

(628) Finally, this is consistent with the result that customers would likely switch to an alternative of RedHawk(-SC) in reaction to a foreclosure strategy by the Merged Entity (see 'First' point above in this sub-Section).

(629) **Third**, customers mix-and-match their EDA tools (i.e., purchase their EDA tools from different vendors across EDA functionalities), precisely because having an integrated portfolio of EDA tools is not the only factor that is important for customers. This suggests that customers would likely not switch to the Merged Entity's EDA tools if the interoperability with third-party EDA tools was totally restricted or degraded.

(630) In the first place, market participants have confirmed the Notifying Party's claim that EDA customers mix-and-match EDA tools across vendors to ensure they have the "best-of-breed" EDA tools for their chip design project. For instance, one market participant noted that "*EDA customers generally source the entire design flow's set of products from each of Synopsys, Cadence and Siemens, and will then mix-and-match the specific EDA tools across vendors according to the needs of the specific chip design. This preference by EDA customers to mix-and-match is driven by the customers' wish to have the best tool for their specific design flow at every*

596 Replies to Questionnaire to customers of EDA and design IP, question C.A.7.1.
597 Minutes of a call with a market participant, dated 14 June 2024, para. 12.
598 Minutes of a call with a market participant, dated 24 June 2024, para. 12.
599 Minutes of a call with a market participant, dated 24 June 2024, para. 10.
600 Replies to Questionnaire to customers of EDA and design IP, question D.B.A.1.
601 Parties' submission to the Commission, "Why Synopsys Could Not Leverage RedHawk to Harm Competitors", 29 August 2024, para. 11, Table 1.

step."[602] Additionally, a competitor submitted that "*the market today favours a mix-and-match, multi-vendor flow with best-in-class solutions. Therefore, Cadence ensures its products can interoperate in third-party environments.*"[603] Moreover, the Commission notes that customers mix-and-match their EDA tools across vendors despite the fact that Cadence and Synopsys have EDA tools that cover all chip design stages, and which can benefit from a deeper, native integration. This is confirmed by the fact that EDA vendors offer their EDA tools on a standalone basis, even when they offer integrated EDA solutions, allowing their customers to mix-and-match EDA tools of their choice. The constant demand for mixing-and-matching shows that having an integrated portfolio of EDA tools (benefiting from native integration) is not as important as other factors in the customer's choice of EDA tools.

(631) In the second place, the market investigation confirmed that quality and technical capabilities are more valued by customers than offering an integrated portfolio of EDA tools. In response to the market investigation, customers rated (i) technical capabilities (average rating 4.7), and (ii) the quality (average rating 4.8) of EDA tools as significantly more important parameters impacting their purchasing strategy and choice of EDA tools, compared to whether an EDA vendor offers a portfolio of integrated EDA tools (average rating 3.4).[604] In response to the market investigation, one customer explained that "*Technical capabilities and quality of EDA tools is of vital importance in order to design out high performance hardware products*." [605] This is confirmed by another customer who emphasised that "*Technical excellence in the semiconductor industry is an absolute requirement. As such, quality and technical capabilities are also required*."[606] Finally, a majority of the respondents considered that this does not differ depending on the type of chip.[607]

(632) In the third place, a majority of customers expressing an opinion confirmed that their choice of other EDA tools used earlier in the chip design process is not influenced by the physical verification and sign-off EDA tools used at the end of the chip design (such as RedHawk(-SC)). In fact, these customers indicated that their choice of physical verification and sign-off EDA tools is independent from their choice of other EDA tools used earlier in the chip design process.[608] In that regard, one customer submitted that while "*Physical verification and sign off EDA tools have an impact on the choice of other EDA tools*", it "*is not the only parameter for the decision.*"[609] Another customer submitted that the selection of EDA tools is based on '*the best technical capabilities independent upon who is providing physical verification and sign-off tools".* [610] Finally, one customer explained that "*in general, we tend to view physical verification and sign-off tools as vendor-agnostic*", meaning that "*the choice of EDA tools does not dictate choice of verification tools and vice-versa".*[611]

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602 Minutes of a call with a market participant dated 24 June 2024, para. 7.
603 Minutes of a call with a market participant, dated 1 July 2024, para. 24.
604 Replies to Questionnaire to customers of EDA and design IP, question C.A.1.
605 Replies to Questionnaire to customers of EDA and design IP, question C.A.2.
606 Replies to Questionnaire to customers of EDA and design IP, question C.A.2.
607 Replies to Questionnaire to customers of EDA and design IP, question C.A.2.
608 Replies to Questionnaire to customers of EDA and design IP, question C.A.3.
609 Replies to Questionnaire to customers of EDA and design IP, question C.A.3.1.
610 Replies to Questionnaire to customers of EDA and design IP, question C.A.3.1.
611 Replies to Questionnaire to customers of EDA and design IP, question C.A.3.1.

(633) **Fourth**, historical examples of tighter integration and greater interoperability between EDA tools demonstrate that this does not necessarily lead to customers switching to those EDA tools.

(634) In the first place, Synopsys' own experience with its integrated product Fusion Compiler demonstrates that tighter integration will not compel customers to switch to an integrated EDA offering. Synopsys launched Fusion Compiler in 2018, natively integrating technologies from some of its most popular products synthesis (Design Compiler), place & route (IC Compiler II), and extraction (StarRC). While Fusion Compiler has [revenue information] since launch, customers [customers' preferences] whose sales [revenue information on tool names] since the launch of Fusion Compiler. Whether a customer wishes to purchase standalone EDA tools or an integrated solution depends on the customer's preference and need at a given time. This variation between customers is supported by the fact that Synopsys' top five customers of its [tool names] products spend differing proportions on each product.[612].[613]

(635) In the second place, this is similarly shown by the fact that Cadence also integrates some of its popular products, while continuing to offer standalone versions of the same tools. For instance, Cadence integrates its gate-level power integrity tool Voltus with its place & route tool Innovus, while customers also purchase those tools standalone. For instance, Ansys estimates that approximately […] of RedHawk(-SC) revenue comes from customers who use it in combination with [tool name].[614]

(636) **Fifth**, the Commission notes that EDA vendors have not generally managed to leverage their strong market position in sign-off EDA markets into other EDA markets, as shown by Synopsys' internal market share estimates illustrated by Figures 9-12 below. Indeed, EDA vendors hold various market positions across EDA markets and various competitors have different areas of strength. This is reflected in the fact that no single EDA vendor can meet all customers' needs and no single EDA vendor is regarded as "best-of-breed" in all stages of the chip design process and for all types of chips design.

(637) In the first place, Siemens' physical verification tool Calibre is the leading EDA tool for physical verification for digital chip design, with an estimated share of approximately [60-70]% market share based on Synopsys' internal estimates in Q2 2024. However, Siemens has not been able to leverage its strong market position physical verification to strengthen its position in neighbouring EDA markets. For example, although physical verification tools are used together with place & route tools, Siemens' presence in place & route is very small (with an estimated share of [0-5]% market share based on Synopsys' internal estimates in Q2 2024).

Figure 9: Siemens' market shares in place & route and physical verification

[…]

Source: Synopsys' estimates ([…]*)*

612 Parties' response to the European Commission's RFI 5, paras. 8.1 and 8.2.
613 Form CO, para. 1038.
614 Parties' response to the European Commission's RFI 14, para. 12.

(638) In the second place, Synopsys' timing analysis tool PrimeTime has a leading position in timing analysis in digital chip design ([90-100]% market share based on Synopsys' internal estimates in Q2 2024). However, Synopsys has not been able to leverage its strong market position timing analysis to strengthen its position in neighbouring EDA markets. For instance, although timing analysis tools are used together with place & route tools, Synopsys' market share in place & route has been declining from [60-70]% (in Q3 2018) to [40-50]% (in Q2 2024) based on Synopsys' internal estimates. In contrast, Cadence's market shares in place & route increased from [30-40]% (in Q3 2018) to [40-50]% (in Q2 2024) based on Synopsys' internal estimates, despite Cadence's timing analysis tool, Tempus, having a substantially lower share than PrimeTime in timing analysis ([10-20]% market share based on Synopsys' internal estimates in Q2 2024). In fact, the worldwide market shares by revenue in 2023 show that Cadence's market share in place & route increased from [40-50]% to [50-60]%, gaining the lead over Synopsys' market share in place & route ([40-50]%).

Figure 10: Synopsys' market shares in place & route and timing analysis ("timing sign-off")

[…]

Source: Synopsys' estimates ([…]*)*

(639) In the third place, the same can be observed in EDA markets circuit simulation and custom layout. Cadence's custom layout tool Virtuoso has a very strong position ([80-90]% market share based on Synopsys' internal estimates in Q2 2024). Despite this, Cadence's market share in circuit simulation ([40-50]% market share based on Synopsys' internal estimates in Q2 2024), a neighbouring EDA market, is lower than Synopsys' ([40-50]% market share based on Synopsys' internal estimates in Q2 2024).

Figure 11: Cadence's market shares in circuit simulation and custom layout

[…]

Source: Synopsys' estimates ([…]*)*

(640) In the fourth place, more generally, the variety of market positions across EDA markets suggests that leveraging market power from one EDA market into another is unlikely.

Figure 12: Estimated market shares across EDA tool categories

[…]

Source: Synopsys' estimates ([…]*)*

(641) **Sixth**, limited instances of termination and/or degradation of interoperability in the past show that (despite the Parties, as well as their rivals, possessing similar or even higher levels of market power) a significant proportion of customers would likely not switch their EDA tool to the Merged Entity's benefit as a result of foreclosure.[615]

615 See Section 5.2 for markets where the Parties' market share has historically exceeded the current market share of Ansys' RedHawk(-SC).

(642) The market investigation confirmed that interoperability restriction is not a regular occurrence in the industry, with only some market participants indicating few instances where a degradation of interoperability occurred. A majority of customers that expressed a view indicated that Synopsys, Ansys, Cadence, Siemens and/or other EDA vendors have not previously terminated/denied, degraded the quality and/or delayed interoperability between their own EDA tools and EDA tools of another vendor (in order to convince customers to switch to its competing EDA tools). More specifically, when asked to explain their answer, the majority of the customers submit that "*they are not aware of any specific cases*" or that "*they have never experienced*" such behaviour.[616] A few customers indicated that Cadence had previously done so, and even fewer that Synopsys had previously done so.[617]

(643) **Seventh**, EDA customers include very large chip design companies with significantly higher turnovers than the Merged Entity (e.g. Nvidia, Intel, Google, Apple), who will likely push back against any foreclosure strategy of the Merged Entity by either switching to competitors' tools or by using their bargaining power to ensure the Merged Entity does not foreclose other EDA vendors. As one customer noted, *'[the customer] has enough countervailing buyer power to "bring them down to earth"'*.[618]

(644) In the first place, as outlined in Section 5.4.5.3.1.2., customers have a significant role in demanding and maintaining effective interoperability, which shows a notable extent of their bargaining power. For instance, the market investigation showed that the majority of customers making a request confirmed that Synopsys, Ansys, Cadence, Siemens and/or other EDA vendors accepted their request to conclude an interoperability agreement with a competing EDA vendor.[619]

(645) In the second place, as explained in the third argument of this Section, customers employ several strategies to increase and maintain their bargaining power vis-à-vis EDA vendors such as mixing-and-matching and multi-homing of EDA tools. For instance, one customer explained that customers pursue different strategies to maintain healthy competition between EDA vendors '*[the customer] fosters competition by supporting smaller companies and startups in various areas, in order to bring its costs down. [The customer] pursues this strategy with its procurement of EDA tools, as well.*'[620], and that '*EDA companies are only aware of each other's tools at a very high level. As a result, whenever a company is becoming more prominent, [the customer] preemptively prevents this by requesting features from competitors and start-ups, ensuring they can fill any gaps. This is not [the customer]-specific as is carried out as well by other market participants such as NVIDIA or Apple.*'[621]

(646) In the third place, there are examples of large customers sponsoring or facilitating entry. For example, [Examples of customer support].[622]

(647) **Finally**, as outlined in Sections 5.4.5.3.1.2.1. and 5.4.5.3.1.2.2., whilst the Commission cannot exclude that the Merged Entity could have the ability to

616 Replies to Questionnaire to customers of EDA and design IP, question C.B.3.1.
617 Replies to Questionnaire to customers of EDA and design IP, question C.B.3.
618 Minutes of a call with a market participant dated 24 June 2024, para. 19.
619 Replies to Questionnaire to customers of EDA and design IP, question C.B.1.
620 Minutes of a call with a market participant dated 24 June 2024, para. 18.
621 Minutes of a call with a market participant dated 24 June 2024, footnote 2.
622 Parties' Response to the CMA Issues Letter of 27 November 2024, para. 7.33.

degrade interoperability between RedHawk(-SC) and third-party timing analysis tools (only Cadence in this case) through proprietary interfaces, the Commission considers that the Merged Entity would likely not have the technical ability to totally restrict interoperability. In other words, the Commission considers that total foreclosure (i.e., entirely removing the interoperability link) is not likely. Whilst partial foreclosure cannot be ruled out, it is in any case only feasible on a limited basis. Therefore, only less extreme forms of foreclosure (on a limited basis) are feasible. In this scenario, the Commission expects less switching away from third-party EDA tools, precisely because the feasible foreclosure strategies are less extreme than in the case of total foreclosure.

(648) Based on the elements considered above, and for the purposes of this Decision, the Commission has reached the conclusion that even if the Merged Entity totally restricted or degraded interoperability between RedHawk(-SC) and third-party EDA tools, it would unlikely have the ability to leverage Ansys' position in the worldwide market for gate-level power integrity with RedHawk(-SC) to foreclose Synopsys' rivals in the EDA markets.

5.4.5.3.1.2.5. Main EDA rivals are able to deploy effective and timely counter-strategies

(649) For the reasons explained below, the Commission considers that, even if the Merged Entity would have the ability to leverage its position, Synopsys' main rivals in the EDA markets and therefore main foreclosure targets, i.e. Cadence and Siemens, would be able to deploy effective and timely counterstrategies in the face of any foreclosure strategy.

(650) **First**, the Commission considers that Synopsys' main EDA rival, Cadence, is a strong EDA competitor that already owns an alternative gate-level power analysis tool and natively integrated EDA tools. Cadence's market position and capabilities make it less dependent on Ansys' EDA tools, including RedHawk(-SC) and able to effectively respond to a potential foreclosure strategy.

(651) In the first place, Cadence offers the second-best alternative gate-level power integrity analysis tool (Voltus) with a [30-40]% market share worldwide in 2023. In addition, Cadence already provides a suite of EDA tools that (natively) integrates Voltus, such as the native integration of Voltus (or a subset of its capabilities) into Cadence's place & route tool Innovus. In fact, Cadence was the first EDA provider to provide a native integration of these tools, in response to which Synopsys and Ansys concluded their partnership to integrate RedHawk(-SC) with Synopsys' EDA tool (RedHawk Analysis Fusion) in 2017.

(652) In the second place, Cadence has established itself as a strong competitor in EDA tools across all chip design types. Further, Cadence has a strong position with respect to EDA tools required for a basic digital chip design: place & route (where Cadence has [50-60]% and Synopsys [40-50]% worldwide in 2023), simulation verification (where Cadence has [30-40]% and Synopsys [30-40]% worldwide in 2023), and parasitic extraction (where each Cadence and Synopsys have [40-50]%worldwide in 2023), but also other EDA tools that interoperate with gate-level power integrity analysis tools such as RedHawk(-SC). Cadence's significant market presence is particularly evident in some EDA markets neighbouring gate-level power integrity analysis, where in 7 out of 12 neighbouring markets Cadence's worldwide market share in 2023 is above 30%, 40% or even 80% (place & route ([50-60]%), simulation verification ([30-40]%), layout ([80-90]%),

parasitic extraction ([40-50]%), characterisation ([40-50]%), emulation-based power analysis ([80-90]%), functional safety & specification analysis ([40-50]%)).

(653) In the third place, as explained in 5.3.3.4.1 above, Cadence has also already been investing in a broad set of capabilities for multi-die chip design, which enable it to retain traction even with the latest chip design trends.

(654) **Second**, the Commission notes that Synopsys' second main rival in EDA, Siemens, also has its own gate-level power integrity analysis tool, as well as strong capabilities in certain EDA markets. Siemens' market position and capabilities make it less dependent on Ansys' EDA tools, including RedHawk(-SC) and able to effectively respond to a potential foreclosure strategy.

(655) In the first place, Siemens offers its own gate-level power integrity analysis tool (mPower) ([5-10]% market share worldwide in 2023). The Commission notes that Siemens launched this tool relatively recently (2021), however the tool already received certification from at least one foundry for its use in the design of digital chips.[623] In addition, in its ordinary course of business, Synopsys and Ansys have been monitoring mPower as an alternative gate-level power integrity analysis tool, which is evident in several of Ansys' internal documents.[624] For instance.[625] [626].[627] in one document Ansys [Ansys' assessment of its competitors]. Further, [Ansys' assessment of its competitors]. In addition, [Ansys' assessment of its competitors]. Another internal Ansys email [Ansys' market intelligence] In addition, [Ansys market intelligence].[628]

(656) In the second place, while Siemens has a smaller presence than Cadence and Synopsys in certain EDA markets and is not active in certain EDA markets where Cadence and Synopsys are present, it is perceived as one of the main competitors in the EDA. As one customer explained '*Synopsys, Cadence and Siemens are top three vendors in the market of EDA tools. Synopsys and Cadence are the 1st and 2nd vendors in the market and Siemens is behind them*'.[629] In addition, one customer explained that in a potential market for EDA tools for analog chip design, '*Cadence and Siemens are the leaders. Synopsys is not significantly present in the market for analog chip design. Whereas Cadence has 42-43 types of tools and Siemens 16-17, Synopsys has only 2 tools and Ansys none in analog chip design (only in simulation)*'.[630] Moreover, Siemens established itself as a leading provider of a physical verification tool Calibre ([60-70]% worldwide in 2023), a critical function for analog and digital chip design.

(657) In the third place, as explained in Section 5.3.3.4.1, Siemens has also already been investing in a broad set of capabilities for multi-die chip design, which enable it to retain traction even with the latest chip design trends.

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623 Siemens website, "Siemens' new mPower Digital solution now certified for GlobalFoundries' platforms", https://newsroom.sw.siemens.com/en-US/siemens-mpower-digital-globalfoundries/, last accessed on 13 December 2024.

624 Form CO, Annex 5.4(c)(SNPS) - 035 - […] and Annex PN RFI 14 - Q.12-003.

625 Form CO, Annex PN RFI 14 Q18.1, slide 4.

626 Form CO, Annex PN RFI 14 Q17.1, slide 1.

627 Form CO, Annex PN RFI 14 Q17.1, slide 1.

628 Parties' response to the European Commission's RFI 14, para. 4.8.

629 Letter addressed to the European Commission, 'Responses to your questions regarding Synopsys and Ansys (Non-Confidential Version), dated 26 June 2024.

630 Minutes of a call with a market participant dated 24 June 2024, para. 13.

(658) **Third**, several market participants considered that the Merged Entity would not be able to foreclose its main competitors in EDA, Cadence and Siemens, since they would have sufficient counter-strategies. For instance, one market participant explained that Cadence does not depend on the Merged Entity because it already has its own gate-level power integrity and integrated offering: '[*customer*] *does not believe that it would be possible for the merged entity to totally remove or degrade interoperability between Ansys' RedHawk(-SC) and any EDA tools developed by its competitors*.' Since '*Cadence has its own solution for EM - IR that competes with Ansys, so there is no obvious reason or motivation for Cadence to consider working with the Merged Entity to have an interoperable solution. They currently do not work with Ansys on an interoperable solution*.' [631] Another market participant considered that in the face of a foreclosure strategy by the Merged Entity '*Other companies in the EDA space (like Cadence and Siemens) would likely continue to offer interoperable solutions. If a merged entity were to limit integration, it could lose market share to competitors who provide more open and flexible solutions*.'[632] Finally, one market participant submitted that the Transaction is a '*defensive move by Synopsys*' in order to enter EDA markets where other EDA companies, such as Cadence and Siemens are already present.[633]

(659) **Fourth**, the Commission considers that mutual dependence for interoperability between EDA vendors (and particularly Cadence and Siemens) gives Synopsys' rivals the possibility to retaliate against any possible foreclosure strategy by the Merged Entity.

(660) In the first place, as already explained in this Section, customers use multiple EDA tools across different functions for their chip design. They do not rely on a single vendor for all the EDA tools they need but rather mix and match software tools from different vendors across the chip design flow. For instance, in 2023, customers representing ~[a significant percentage]% of Synopsys' sales used EDA tools from different vendors. EDA software tools of different vendors therefore must interoperate and enable the data from one vendor's EDA tool to be read by an EDA tool of another vendor.

(661) In the second place, the Commission notes that Synopsys and Ansys have each concluded extensive interoperability agreements to collaborate with their EDA competitors and improve interoperability between their products ("flows")[634], primarily at their customers' demand. These partnerships involve cross-licensing of each partner's respective software products and the development of joint solutions to facilitate data transfer between EDA tools. By means of interoperability agreements, EDA vendors grant courtesy access to their EDA tools such that each partner to the agreement may perform the necessary tests and provide support. For instance, Synopsys has around [a significant number] supported interoperability flows with Siemens, covering more than [a significant number] Siemens tools, and more than [a significant number] supported interoperability flows with Cadence,

631 Replies to Questionnaire to customers of EDA and design IP, question D.B.A.5.

632 Replies to Questionnaire to customers of EDA and design IP, question D.B.A.8.1.

633 Minutes of a call with a market participant dated 24 June 2024, para. 17.

634 All interoperability agreements are concluded at "flow" level. Flows involve one or more tools of Synopsys/Ansys and the relevant third party. Interoperability agreements specifically call out the EDA tools that form part of the "flow".

which enable Synopsys to access EDA tools of Cadence and Siemens.[635] Since customers frequently use Synopsys EDA tools in the chip design process alongside Cadence and Siemens tools as described below, the Merged Entity will likely continue depending on the established interoperability agreements post-Transaction.

(662) In that respect, several Synopsys' internal documents available to the Commission show that the Parties' customers mix-and-match EDA tools of Cadence and Siemens with Synopsys' EDA tools and demand interoperability improvements between their EDA tools. For instance:

(a) One internal document shows [customer request for interoperability with third party tools].[636]

(b) Another internal document shows an instance where [customer request for interoperability with third party tools].[637]

(663) In addition, several Synopsys' internal documents available to the Commission show that Synopsys depends on Cadence and Siemens to address their customers' demand for improved interoperability. For instance:

(a) [Example of Synopsys' interoperability collaboration with EDA vendor][638]

(b) Another internal document reflects [customer request for interoperability with third party tool [639]

(664) In the third place, the Parties' main EDA rivals, Cadence and Siemens have a strong or leading position in several EDA markets and their EDA tools are widely used by customers in conjunction with the Merged Entity's own EDA tools, including RedHawk(-SC). It is therefore reasonable to expect that the Merged Entity will continue to depend on collaborating with Cadence and Siemens to satisfy their customers' demand for an improved interoperability. In consequence, in response to a potential foreclosure strategy, Cadence and Siemens could retaliate by restricting or degrading interoperability with their own successful EDA tools and products for chip design.

(665) More specifically:

(a) Cadence is a significant player in many EDA markets. For instance, with respect to EDA tools for digital chip design, Cadence has more than [40-50] % market share worldwide in 2023 in at least 7 different EDA market segments. With respect to EDA tools for analog chip design, Cadence has more than [80-90]% market share worldwide in 2023 in at least 5 different EDA market segments. In view of their competitiveness, Synopsys' customers widely use Cadence's EDA tools alongside Synopsys'. For instance, according to […] Synopsys, [Synopsys market intelligence][640].[641].

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635 Parties' response to the European Commission's RFI 22, para. 5.10. Counting of interoperability flows as of 31 August 2024. Form CO, para. 1072.

636 Annex PN RFI 22 Q. 14.010.

637 Annex PN RFI 22 Q. 14.006.

638 Annex PN RFI 22 Q. 14.007.

639 Annex PN RFI 22 Q. 14.008.

640 Form CO, para. 1106. Annex PN RFI 3 Q.3(v).

641 [Synopsys market intelligence].

(b) Siemens is a leading supplier of EDA tools for physical verification (with its tool Calibre), an EDA tool functionality that is necessary for designing a basic digital or analog chip. Based on Synopsys'[data], [Synopsys market intelligence].[642]

(666) In that respect, the Commission notes that Synopsys' interoperability agreements with Cadence and Siemens include licenses for access to their most popular EDA tools.[643] This further gives Cadence and Siemens the possibility to retaliate by restricting or degrading Synopsys' license to their EDA tools, in response to any foreclosure strategy. In particular: [Cadence's and Siemens' tools licensed to Synopsys under their respective interoperability agreements].[644]

(667) Finally, the Commission notes that the CEO of Synopsys' biggest rival, Cadence, which would likely be impacted the most by any such foreclosure strategies, publicly noted that '*we are still pretty differentiated in terms of Analysis, still very differentiated because we have the broadest EDA portfolio with analog and digital. And then, of course, we have a critical piece of packaging that drives 3D-IC*'. In consequence, the CEO of Cadence considered that the Transaction does not '*change the competitive landscape in any big way.*',[645] and that Synopsys is '*trying to react to what [Cadence] did like 6 years ago*'.[646]

(668) On the basis of all these elements, and for the purposes of this Decision, even if the Merged Entity would have the ability to leverage its position, Synopsys' main rivals in the EDA markets, Cadence and Siemens, would be able to deploy effective and timely counterstrategies in the face of any foreclosure strategy.

5.4.5.3.1.2.6. Conclusion on the Merged Entity's ability to foreclose competing providers of EDA tools by totally restricting or degrading interoperability between RedHawk(-SC) and third-party EDA tools

(669) On the basis of all these elements, and for the purposes of this Decision, the Commission considers it **unlikely that the Merged Entity would have the ability** to engage in a strategy of market-wide foreclosure of competing providers of EDA tools by totally restricting or degrading interoperability between RedHawk(-SC) and third-party EDA tools in any of the affected interoperability pairings relating to Ansys' tools in gate-level power integrity specified in Annex A of the Decision.

642 Form CO, para. 1107. Annex PN RFI 3 Q.3(v).

643 Parties' response to the European Commission's RFI 23, para. 4.2.

644 Annexes PN RFI 1 Q.20-45.

645 JPMorgan Conference, May 21, 2024, Annex RFI4Q15(SNPS) – 11(EC RFI 3 – Consolidated Response).

646 JPMorgan Conference, May 21, 2024, Annex RFI4Q15(SNPS) – 11(EC RFI 3 – Consolidated Response) / Annex PN RFI 3 Q.6(i) and (ii) ("Yes, we are very well positioned. I mean, I think the other people are trying to reach to what we did like 6 years ago. So there's no need to react to the reaction."). Cadence has also noted that it has an "advantage in making and being early" in that it has had to spend significantly less than the Synopsys acquisition price to develop its portfolio. John M. Wall, Cadence Senior VP & CFO, Interview at NASDAQ Investor Conference, June 11, 2024, transcript submitted in RFI4Q15(SNPS) – 11(EC RFI 3 – Consolidated Response) / Annex PN RFI 3 Q.6(i) and (ii).

5.4.5.3.1.3. The Merged Entity's ability to foreclose competing providers of EDA tools by engaging in anti-competitive bundling

(670) For the reasons explained below, the Commission considers that the Merged Entity would not have the ability to engage in a strategy of market-wide foreclosure of competing providers of EDA tools by engaging in anti-competitive (pure and/or mixed) bundling between RedHawk(-SC) and third-party EDA tools.

(671) That finding is without prejudice to the fact that, as noted in Section 5.4.1. many EDA tools are purchased by the same set of customers (either together or separately) to perform complementary tasks. Therefore, many EDA tools in the chip design flow are interrelated and complementary in nature, and thereby could potentially be sold together in a bundle. Although the Commission cannot exclude that the Merged Entity may theoretically have the possibility to bundle any of its EDA tools together, either with pure bundling or with mixed bundling, the Commission considers that in reality the Merged Entity would not have the ability to foreclose competing providers of EDA tools by engaging in anti-competitive bundling the following reasons.

(672) **First**, it is unlikely that a significant proportion of customers would switch their EDA tool as a result of the Merged Entity engaging in anti-competitive (pure and/or mixed) bundling between RedHawk(-SC) and Synopsys EDA tools.

(673) In the first place, in response to the market investigation, customers rated (i) the fact that the provider offers a portfolio of (integrated) EDA tools and/or related products (e.g., design IP, TCAD, etc.), (ii) familiarity with the EDA tools of a given EDA vendor, and (iii) EDA vendor reputation as the least important parameters impacting their purchasing strategy and choice of EDA tools, whilst technical capabilities and quality were the most important.[647] This suggests that customers do not value bundles, but rather value the specific EDA tools within a bundle on their merit. This indicates that customers would unlikely switch (i.e. move away from competitors' EDA tools to the Merged Entity's) in reaction to the Merged Entity engaging in anti-competitive bundling.

(674) In the second place, as outlined in Section 5.4.5.3.1.2.4. above, customers mix-and-match their EDA tools across vendors, as well as multi-home (i.e. use at least two EDA vendors for one tool functionality), despite many EDA vendors already offering discounts for bundles. This again suggests that customers do not value bundles, but rather value the specific EDA tools within a bundle on their merit. This indicates that customers would unlikely switch (i.e. move away from competitors' EDA tools to the Merged Entity's) in reaction to the Merged Entity engaging in anti-competitive mixed bundling.

(675) In the third place, a majority of customers during the market investigation indicated that the Parties have not previously refused to sell an EDA tool on a standalone basis in order to convince the customer to purchase a bundle of their EDA tools, i.e., pure bundling. Instead, a limited number of customers indicated the Parties have previously engaged in certain forms of mixed bundling, where the standalone products were sold a higher combined price than the bundle.[648]

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647 Replies to Questionnaire to customers of EDA and design IP, question C.A.1.

648 Replies to Questionnaire to customers of EDA and design IP, question C.C.1 and C.C.1.1.

(676) In the fourth place, there is no evidence to suggest that the historical instances of mixed bundling led to significant changes in market shares, despite mixed bundling being a common practice in this industry. Indeed, the Commission understands that EDA tools, as a software product, have a very low marginal cost, and therefore EDA vendors have an incentive to offer bundles or additional EDA tools at a low cost. However, even despite mixed bundling being a common practice in the industry, there are still EDA markets where Cadence and Synopsys, which have the broadest portfolio of products across the chip design flow, still have low market shares. Meanwhile the individual "point" EDA tools of Siemens, Ansys or other EDA vendors remain strong, even though they are not able to offer similar bundles.

Figure 13: Estimated market shares across EDA tool categories

[…]

Source: Synopsys' estimates ([…]*)*

(677) **Second**, it does not appear that Synopsys has refused to sell its EDA tools on a standalone basis following previous acquisitions. The Commission understands that following past acquisitions, Synopsys continued to sell EDA tools standalone, unless the capabilities of acquired tools overlapped with Synopsys' products and/or there was no customer demand for the given EDA tool to be sold standalone. Further, market participants indicated only a limited number of instances where Synopsys stopped selling EDA tools standalone, which related to Synopsys' acquisition of a company called Dorado in 2020. Following the acquisition of Dorado, in 2022, Synopsys launched a new tool called PrimeClosure that integrated capabilities from Dorado's former Tweaker tool. After releasing the successor product PrimeClosure, Synopsys decided to de-emphasize Tweaker, which meant that the product continued to be sold to existing customers but no longer to new customers.[649] However, the Commission understands that Synopsys has not received any requests to purchase Tweaker from new customers, and that approximately [a significant percentage]% of existing Tweaker customers have chosen to migrate to the new product PrimeClosure. Further, [a limited number] existing Tweaker customers extended their Tweaker licenses so far, to address their specific needs.[650].[651]

(678) **Third,** the Parties' EDA rivals also sell their EDA tools on a standalone basis even though they already have a full range of offerings. For example, Cadence continues to offer gate-level power integrity tool Voltus and place & route tool Innovus on a standalone basis (despite offering a solution that integrates the two EDA tools). In addition, [a significant percentage] of RedHawk(-SC) revenue comes from customers who use it in combination with [tool name]tool.[652] Voltus and Innovus are the equivalent of Ansys' RedHawk(-SC) and Synopsys' EDA tools, and so this suggests the Merged Entity would similarly continue to sell these EDA tools on a standalone basis, without engaging in pure bundling, post-Transaction.

(679) **Fourth**, as outlined in Section 5.4.5.3.1.2.5, the Commission considers that even if the Merged Entity would have the ability to leverage its position, Synopsys' main rivals in the EDA markets, Cadence and Siemens, would be able to deploy

649 Parties' response to the European Commission's RFI 25, para. 26.5.
650 Parties' response to the European Commission's RFI 25, para. 26.7.
651 Parties' response to the European Commission's RFI 25, para. 26.9.
652 Parties' response to the European Commission's RFI 14, para. 12.

effective and timely counterstrategies in the face of any foreclosure strategy. Similarly, the Commission considers that, in light of the strength and breadth of products of Cadence and Siemens, Synopsys' rivals would be able to retaliate against the Merged Entity's bundling with similar bundles of their own.

(680) On the basis of all these elements, and for the purposes of this Decision, the Commission has reached the conclusion that the Merged Entity would not have the ability to engage in a strategy of market-wide foreclosure of competing providers of EDA tools by means of anti-competitive (pure and/or mixed) bundling between RedHawk(-SC) and third-party EDA tools in any possible bundle pairings.

5.4.5.3.1.4. Conclusion on the Merged Entity's ability to foreclose competing providers of EDA tools by leveraging Ansys' gate-level power integrity tool RedHawk(-SC)

(681) On the basis of all these elements, and for the purposes of this Decision, the Commission concludes that the Merged Entity **would not have the ability** to engage in a strategy of market-wide foreclosure of competitors in EDA markets by totally restricting or degrading interoperability in any of the affected interoperability pairings relating to Ansys' tools in gate-level power integrity specified in Annex A of the Decision, or by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings.

5.4.5.3.2. Incentive to foreclose

(682) For the reasons set out below, the Commission has reached the conclusion that the Merged Entity **would not have the incentive** to engage in a strategy of market-wide foreclosure of competitors in EDA markets by totally restricting or degrading interoperability in any of the affected interoperability pairings relating to Ansys' tools in gate-level power integrity specified in Annex A of the Decision, or by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings.[653]

(683) When considering whether or not to engage in such practices, the Merged Entity faces a trade-off between forgone sales of RedHawk(-SC) and additional or retained sales of Synopsys EDA tools that could otherwise have gone to Synopsys' rivals.

(684) **First**, as outlined in Section 5.4.5.3.1.2.4, it is unlikely that a significant proportion of customers would switch to Synopsys' EDA tools as a result of totally restricting or degrading interoperability or anticompetitive (pure and/or mixed) bundling. In this event, the Merged Entity would make limited additional sales of Synopsys EDA tools, and therefore not make significant additional profits from such a foreclosure strategy.

(685) **Second,** as outlined in Section 5.4.5.3.1.2.4 , a majority of customers expressing a view during the market investigation indicated that, in response to such foreclosure strategy, they would switch to an alternative of RedHawk(-SC) (rather than switch to a Synopsys EDA tool that continues to interoperate with RedHawk(-SC)).[654] In

653 Except for when it specifically relates to interoperability, the Commission's assessment of the Merged Entity's incentive to leverage Ansys' potentially strong market position in gate-level power integrity to foreclose EDA competitors also applies to a potential concern of anticompetitive (pure and/or mixed) bundling.

654 Replies to Questionnaire to customers of EDA and design IP, question D.B.A.10.

this event, the Merged Entity would forgo significant sales of RedHawk(-SC), and therefore incur losses from such a foreclosure strategy.

(686) **Third**, the Commission notes that some interoperability pairings based on proprietary interfaces are not used by a significant proportion of customers, because they are an optional step required only for a specific use case. This is also the case with the link between gate-level power integrity tools and timing analysis tools, where less than [a small percentage]% of customers that use timing analysis tools use it in combination with a gate-level power integrity tool. While timing analysis is a critical function for the design of digital chips, its interoperability link with gate-level power integrity is optional. In other words, [a significant percentage] customers do not use this interoperability link at all.[655] Such interoperability pairings would not allow the Merged Entity to influence the behaviour of a significant proportion of customers and make a realistic profit from any foreclosure strategy.

(687) **Fourth**, as outlined in Section 5.4.5.3.1.2.5, the Merged Entity's competitors, i.e. Cadence and Siemens, have the ability to deploy effective and timely counter-strategies to any such foreclosure strategy. Thus, it is unlikely that the Merged Entity could use such foreclosure strategy to gain and/or protect a strong market position against Cadence and Siemens in the long-term. Therefore, such foreclosure strategy would likely not be dynamically profitable in the long-term, since it is unlikely that the Merged Entity could recoup any short-term losses with long-term gains.

(688) **Fifth**, the fact that the Merged Entity would not have the incentive to engage in such a foreclosure strategy is consistent with the lack of evidence of similar foreclosure strategies having been implemented in the past, despite the fact that Synopsys has a strong market position in many EDA markets and is active across the EDA chip design flow.

(689) In the first place, a majority of the customers that expressed a view in the market investigation confirmed the Parties have never terminated/denied, degraded the quality and/or delayed interoperability between their own EDA tools and the EDA tools of rivals (in order to convince the customer to switch to the Parties' competing EDA tools).[656] Despite the observation of one market participant who submitted that '*Synopsys, as it grew through acquisitions to become the leader in EDA, has gradually shifted to a closed model based on tool integration and degradation of interoperability of the standalone versions of its tools with those of third parties*'[657], the market investigation showed only a few customers indicating that Synopsys had previously done so.[658] The limited number of instances where customers confirmed this had occurred related to Synopsys' acquisition of Dorado and its EDA tool called Tweaker in 2020. Two market participants indicated that following Synopsys' acquisition of Dorado in 2020, Synopsys has restricted interoperability with the acquired tool called Tweaker. In addition, according to

655 Parties' response to the European Commission's RFI 25, paras. 19.4-19.5.

656 Replies to Questionnaire to customers of EDA and design IP, question C.B.3 and C.B.3.1.

657 Market participant's response to the CMA's RFI of 21 October, question 6.

658 Replies to Questionnaire to customers of EDA and design IP, question C.B.3. Similarly, few customers indicated that Cadence had previously done so. This is consistent with the Merged Entity not having the incentive to engage in such a foreclosure strategy, because Cadence (similar to Synopsys) has a strong market position in many EDA markets and is active across the EDA chip design flow.

one market participant, Synopsys started introducing new features to the Tweaker tool that were delayed or even not implemented in flows with rival EDA tools.[659] In that respect, the Notifying Party submitted that, prior to Synopsys' acquisition of Dorado, Tweaker interoperated with third-party EDA tools through industry standards and that the support for those formats has not changed post-acquisition. However, the Commission notes that, as outlined in Section 5.4.5.3.1.3, following the acquisition of Dorado, in 2022, Synopsys launched a new tool called PrimeClosure that integrated capabilities from the Tweaker tool; this new tool was heavily favoured by customers, which chose themselves to switch to this tool. On the complaints by customers and competitors, while the Notifying Party admitted that Synopsys has received some complaints about interoperability issues and stability of PrimeClosure (the successor of Tweaker) from their customers, it confirmed that Synopsys resolved all the issues it was made aware of.[660] In addition, the Notifying Party confirmed that Synopsys has not received complaints from customers or EDA competitors about delayed releases of new features of Tweaker/PrimeClosure in their flow with competing EDA tools.[661]

(690) In the second place, a majority of the customers that expressed a view confirmed the Parties have never denied their request to conclude an interoperability agreement with a competing EDA vendor.[662]

(691) In the third place, a majority of the customers that expressed a view confirmed the Parties have never refused to (continue to) sell the customer an EDA tool on a standalone basis (in order to convince the customer to purchase a bundle of the Parties' EDA tools).[663] The limited number of instances where customers confirmed this had occurred related to offering the future releases of the tool as part of a package or increasing the price of a standalone product compared to when the tool is sold in a bundle. However, several customers also noted that, as a common industry practice, all EDA vendors offer bundles of EDA tools at lower price, with customers usually negotiating the price and flexibility of the bundle with the EDA vendors. For instance, one customer explained that '*Bundling multiple tools into a new product is a common practice and is often used to increase prices in the new contract.*'; and another customer explained that '*Bundling and repackaging is common practice. […] The solution is usually to discuss the price and flexibility offered with the new bundles*.'[664]

(692) In the fourth place, as outlined in Section 5.4.5.3.1.2.4, Synopsys' past experience with its integrated product […] demonstrates that tighter integration of EDA tools does not mean significant number of customers will switch to those tools. [Details of the Synopsys integrated product, which combines capabilities offered by several other Synopsys tools]. However, customers continue to use the standalone versions of these tools and their sales have continued increasing since the launch of […].[665] This suggests that the Merged Entity would not be able to fully profit from fully integrating their EDA tools (either through interoperability restriction or

659 Replies to Questionnaire to customers of EDA and design IP, question C.B.3.1.
660 Parties' response to the European Commission's RFI 25, para. 26.16.
661 Parties' response to the European Commission's RFI 25, para. 26.22.
662 Replies to Questionnaire to customers of EDA and design IP, question C.B.2 and C.B.2.1.
663 Replies to Questionnaire to customers of EDA and design IP, question C.C.1 and C.C.1.1.
664 Replies to Questionnaire to customers of EDA and design IP, question C.C.1 and C.C.1.1.
665 Parties' response to the European Commission's RFI 5, paras. 8.1 and 8.2.

degradation of rivals' EDA tools or bundling of their own products), because a significant proportion of customers would still prefer standalone products.

(693) **Sixth**, as outlined in Section 5.4.3.1.2, interoperability is an important element of the EDA markets, whose features of supply and demand generally incentivize EDA vendors to maintain effective interoperability. Given the extent to which customers mix-and-match EDA tools of different vendors, the EDA tools' attractiveness depends on its ability to interoperate with any EDA tool that a customer selects. This in turn suggests that there are gains to be made from increasing the interoperability of your EDA tools with third party EDA tools, i.e. by increasing the quality of your EDA tools as well as those of complementary third-party EDA tools. Conversely, this suggests that totally restricting or degrading the interoperability of one company's EDA tools would result in losses. This is particularly true for RedHawk(-SC), which interoperates with several different EDA tool functionalities based on the same industry-standard file format. Totally restricting or degrading RedHawk(-SC)'s support for a given industry standard would impact its interoperability with any EDA tool that interchanges with RedHawk(-SC) and aggravate the Merged Entity's potential losses in the face of this strategy.

(694) **Finally**, as outlined in Section 5.4.5.3.1.2.4, EDA customers include very large chip design companies with significantly higher turnovers than the Merged Entity (e.g. Nvidia, Intel, Google, Apple), who will likely push back against any foreclosure strategy of the Merged Entity by either switching to competitors' tools or by using their bargaining power to ensure the Merged Entity did not foreclose other EDA vendors. In that respect, one customer observed that '*the Parties will not have an incentive to [degrade the interoperability of their EDA tools with third-party tools] post-Transaction, because there would be push-back from customers, who prefer a mix-and-match approach to sourcing their EDA tools for their design flows, which necessitates interoperability between vendors' EDA tools.*'[666]

(695) In light of the above, the Commission concludes that the Merged Entity **would not have the incentive** to engage in a strategy of market-wide foreclosure of competitors in EDA markets by totally restricting or degrading interoperability, in any of the affected interoperability pairings relating to Ansys' tools in gate-level power integrity specified in Annex A of the Decision, or by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings.

5.4.5.3.3. Impact on effective competition

(696) Given that the Commission has reached the conclusion that the Merged Entity would neither have the ability nor the incentive to engage in a strategy of market-wide foreclosure of competitors in EDA markets by totally restricting or degrading interoperability in any of the affected interoperability pairings relating to Ansys' tools in gate-level power integrity specified in Annex A of the Decision, or by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings, the Commission has not assessed whether the impact of such foreclosure strategies would lead to a significant impediment to effective competition. However, the following evidence indicates that the effect would in any case be limited.

666 Minutes of a call with a market participant dated 24 June 2024, para. 18.

(697) **First**, as outlined in Section 5.4.5.3.1.2.1. and 5.4.5.3.1.2.2., whilst the Commission cannot exclude that that the Merged Entity could have the ability to degrade interoperability between RedHawk(-SC) and third-party timing analysis tools through proprietary interfaces, the Commission considers that the Merged Entity would likely not have the technical ability to restrict interoperability. In other words, the Commission considers that total foreclosure (i.e., entirely removing the interoperability link) is not likely, whilst partial foreclosure cannot be ruled out, but in any case is only feasible on a limited basis. Therefore, only less extreme forms of foreclosure (on a limited basis) are feasible. In this scenario, the Commission expects a more limited effect on competition, precisely because the feasible foreclosure strategies are less extreme than in the case of total foreclosure.

(698) **Second**, the conclusion that there will not be any appreciable negative impact on customers is furthermore confirmed by the results of the market investigation. The majority of customers consider that the impact of the Transaction on their company would be positive or neutral and that the impact of the Transaction on the relevant EDA markets would be positive or neutral.[667] Moreover, several customers proactively reached out to the Commission to express their support for or neutrality towards the Transaction.[668]

(699) **Third**, the impact of the potential restriction or degradation of interoperability would be limited with respect to some affected interoperability pairings simply because RedHawk(-SC) is not presently used in combination with specific rivals' EDA tools. More precisely, in two affected interoperability pairings (gate-level power integrity to RTL power consumption analysis; and gate-level power integrity to functional safety & specification analysis), [Name of vendor] EDA tools have no actual data import and export relationship with RedHawk(-SC). [Customer usage of RedHawk (-SC) in combination with the vendor's tools*]*.[669]

5.4.5.3.4. Conclusion

(700) In view of the above considerations and in light of the results of the market investigation and the evidence and information available to it, the Commission concludes that the Transaction does not raise serious doubts as to its compatibility with the internal market as a result of conglomerate effects, notably by foreclosing competing providers of EDA tools through leveraging of Ansys' Redhawk(-SC), considering that the Merged Entity would not have the ability and incentive to engage in such strategy.

5.4.6. Leveraging from Ansys' position in the market for electromagnetic simulation (HFSS) to foreclose Synopsys' rivals in the EDA markets

5.4.6.1. Potential concern

(701) The Commission has assessed a potential competition concern whereby the Merged Entity would have the ability and incentive to leverage Ansys' potentially strong position in a worldwide market for *electromagnetic simulation* (with its tool HFSS), where Ansys has [50-60]% market share worldwide by revenue in 2023,

667 Replies to Questionnaire to customers of EDA and design IP, question E.2-E.5.

668 Letters from customers to the European Commission in relation to Case M.11481, dated 16 July 2024, 23 July 2024, 30 July 2024, 31 July 2024, 16 August 2024, 22 August 2024, 6 September 2024 and 16 October 2024

669 Parties' response to the European Commission's RFI 14, para. 5.4.

into neighbouring EDA markets (based on both interoperability pairings and bundle pairings) where Synopsys is active, and whether such a foreclosure strategy would have a significant detrimental effect on competition in the relevant markets.

(702) In that regard, one market participant indicated that Ansys has a leading electromagnetic simulation tool HFSS, which it offers on a standalone basis, with effective interoperability based on open APIs with third-party EDA tools, consistent with its "Swiss-neutral" approach. [670] According to the market participant, Ansys has consistently ensured that their tools can seamlessly interoperate with third-party tools while Synopsys has a documented history of degrading interoperability with its standalone tools. In the same vein, the Merged Entity will have the ability to delay, degrade or entirely restrict interoperability with the standalone versions of HFSS to drive customers towards its integrated solution.[671] The participant explained that the Merged Entity would also have the ability to integrate Ansys' tools (including HFSS) in its integrated offering and to engage in mixed bundling.[672] According to the market participant, Synopsys will also have the incentive to foreclose competitors, in particular in relation to tools that interoperate with Ansys' HFSS and that are critical for the chip design (e.g., timing and signal integrity, place & route, power integrity).[673]

(703) Therefore, as outlined in Section 5.4.3., the Commission has assessed two potential concerns relating to Ansys' electromagnetic simulation tool HFSS: (i) total restriction or degradation of interoperability between HFSS and third-party EDA tools and (ii) anticompetitive (pure and/or mixed bundling) with Ansys' HFSS and Synopsys' products. The specific foreclosure mechanisms assessed are equivalent to those outlined in Sections 5.4.5.1.

5.4.6.2. The Notifying Party's view

(704) For the same reasons as outlined in Section 5.4.4, the Notifying Party submits that the Merged Entity will lack the ability and the incentive to leverage Ansys' electromagnetic simulation tool HFSS to foreclose competitors in the EDA markets by degrading/removing interoperability or by means of anticompetitive bundling/tying, and that any foreclosure strategy would not significantly impede effective competition.

5.4.6.3. The Commission's assessment

5.4.6.3.1. Ability to foreclose

(705) For the reasons set out below, the Commission has reached the conclusion that the Merged Entity **would likely not have the ability** to engage in a strategy of market-wide foreclosure of competing providers of EDA tools by totally restricting or degrading interoperability between HFSS and third-party EDA tools in any of the affected interoperability pairings relating to electromagnetic simulation tools specified in Annex A of the Decision, or by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings.

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670 Market participant's submission to the European Commission dated 14 June 2024, paras. 105 and 118.

671 Market participant's submission to the European Commission dated 14 June 2024, paras. 119, 122 and 126.

672 Market participant's submission to the European Commission dated 14 June 2024, para. 129.

673 Market participant's submission to the European Commission dated 14 June 2024, paras. 130-133.

(706) **First**, the Commission cannot exclude that HFSS holds a significant degree of market power on the worldwide market for electromagnetic simulation (Section 5.4.6.3.1.1). **Second**, the Commission considers that the Merged Entity would likely not have the ability to foreclose competing providers of EDA tools by totally **restricting** or degrading interoperability between HFSS and third-party EDA tools (Section 5.4.6.3.1.2). **Third**, the Commission considers that the Merged Entity would likely not have the ability to foreclose competing providers of EDA tools by engaging in anti-competitive (pure and/or mixed) bundling between HFSS and Synopsys' EDA tools (Section 5.4.6.3.1.3).

5.4.6.3.1.1. Assessment of Ansys' potential market power in the worldwide market for electromagnetic simulation

(707) For the reasons explained below, **the Commission cannot exclude that Ansys holds a significant degree of market power** on the worldwide market for electromagnetic simulation with its tool HFSS. This is because, whilst the market investigation showed that there are some relevant alternatives to HFSS, it remains the leading product on the market in terms of market share and is often singled out for its strength and quality.

(708) **First**, the Commission notes that Ansys holds a significant market share in a global market for electromagnetic simulation with HFSS: [50-60]% worldwide by revenue in 2023. The only other providers of electromagnetic simulation tools are Cadence (Clarity; EMX; [30-40]% worldwide by revenue in 2023), Keysight (Pathwave EM Design – EMPro, RFPro; [10-20]% worldwide by revenue in 2023) and Dassault (CST Studio Suite; [0-5]% worldwide by revenue in 2023*)*.

(709) **Second,** HFSS is widely considered by market participants as a "golden standard" tool, with few effective alternatives. For instance, one customer explained that "*Ansys tools have always been best-in-class in this area*". A second customer stated that "*HFSS is a gold standard EM simulator that only has direct competition in Cadence Clarity and Keysight Pathwave/ADS".* A third customer explained that"*HFSS can to certain extent be replaced by tools from e.g. Keysight. However some features are unique".* A fourth customer stated in relation to HFSS that "*no good alternatives exist today*".[674] A fifth customer explained that "*HFSS does have competitors, but they either lack some required features (...) or are not very mature (..)".*[675]

(710) **Third**, the Commission's market investigation has shown that the alternatives to Ansys' HFSS are considered less established and less mature. For instance, one customer explained that "*Cadence is an up and comer [sic] but solutions lack the cohesiveness that Ansys solutions provide."* A second customer stated that "*the Cadence tools are less established and not as mature*." A third customer explained that *"(t)he HFSS is a long established tool".*[676]

(711) **Fourth,** Ansys' strong position in electromagnetic simulation is also reflected in the internal documents of Synopsys and Ansys, [competitive assessment of HFSS].[677].[678]

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674 Replies to Questionnaire to customers of EDA and design IP, question D.A.F.3.1.

675 Replies to Questionnaire to customers of EDA and design IP, question D.B.C.13.

676 Replies to Questionnaire to customers of EDA and design IP, question D.A.F.3.1.

677 Form CO, Annex 5.4(c)(SNPS) – 035.

(712) On the basis of all these elements, and for the purposes of this Decision, the Commission cannot exclude that Ansys has a significant degree of market power in the worldwide market for electromagnetic simulation with its HFSS tool.

5.4.6.3.1.2. The Merged Entity's ability to foreclose competing providers of EDA tools by totally restricting or degrading interoperability between HFSS and third-party EDA tools

(713) For the reasons explained below, the Commission considers it **unlikely that** the Merged Entity **would have the ability** to engage in a strategy of market-wide foreclosure of competing providers of EDA tools by totally restricting or degrading interoperability between HFSS and third-party EDA tools in any of the affected interoperability pairings relating to electromagnetic simulation tools specified in Annex A of the Decision.

(714) **First**, the Merged Entity would likely not have the technical ability to *totally restrict or even degrade* interoperability between HFSS and third-party EDA tools, because interoperability is presently based exclusively on industry-based standard interfaces (Section 5.4.6.3.1.2.1). **Second**, even if it was possible to technically totally restrict or degrade interoperability, the Merged Entity would unlikely engage in this foreclosure mechanism to foreclose its EDA rivals (Section 5.4.6.3.1.2.2). **Third**, even if the Merged Entity totally restricted or degraded interoperability between HFSS and third-party EDA tools, the Commission considers that the Merged Entity would not have the ability to leverage Ansys' position in the market for electromagnetic simulation with HFSS, because it is unlikely that a significant proportion of customers would switch to EDA tools of the Merged Entity as a result of foreclosure of third-party EDA tools (Section 5.4.6.3.1.2.3). **Fourth**, even if the Merged Entity would have the ability to leverage its position in the market for electromagnetic simulation, the Commission considers that Synopsys' main rivals in the EDA markets would be able to deploy effective and timely counterstrategies in the face of any foreclosure strategy (Section 5.4.6.3.1.2.4).

5.4.6.3.1.2.1. Technical ability to hamper interoperability between HFSS and third-party EDA tools

(715) As the table below shows, HFSS imports data from or exports data to third-party EDA tools exclusively based on industry-standard file formats. HFSS currently does not interoperate with third-party (non-Synopsys) EDA tools based on proprietary interfaces, and the Commission understands that Ansys had no plans to establish such interoperability.

678 Form CO, Annex 5.4(c)(SNPS) – 040; Annex 5.4(ab)(SNPS) – 016; Annex 5.4(c)(SNPS) – 035

Table 45: Interoperability between Ansys' electromagnetic simulation tool HFSS and third-party (non-Synopsys) EDA tools

Data flow direction	Function of third-party (non-Synopsys) EDA tools that interoperate with Ansys' electromagnetic simulation tool (HFSS)	Interoperability format
HFSS imports from	Layout	Industry standards
HFSS imports from	Photonic layout design implementation	Industry standards
HFSS exports to	Circuit simulation	Industry standards
HFSS exports to	Layout	Industry standards

(716) Given that HFSS presently interoperates with third-party (non-Synopsys) EDA tools solely based on industry-standards and not proprietary interfaces, the Commission will only assess the Merged Entity's technical ability to totally restrict or degrade this baseline interoperability between HFSS and third-party EDA tools but will not separately discuss such ability with respect to interoperability based on proprietary interfaces.

(717) **As regards the Merged Entity's technical ability to totally restrict or degrade interoperability between HFSS and third-party EDA tools ensured through industry-standard file formats (i.e., baseline interoperability)**, the Commission considers that the Merged Entity would likely not have such an ability, for the following reasons.

(718) **First**, for the reasons mirroring those provided in Section 5.4.5.3.1.2.1, the Commission's market investigation confirmed that the Merged Entity would unlikely have the ability to totally restrict or degrade the baseline interoperability between HFSS and third-party EDA tools.

(719) As already explained in Section 5.4.5.3.1.2.1. b), EDA suppliers have a very limited scope to hamper interoperability based on industry-standard file formats. To validate their tools' compatibility with industry-standard file formats, EDA vendors perform unilateral checks on their respective tools by relying on specifications and manuals published by the standards committee or industry consortium that maintains the standard in question. Therefore, the EDA vendor's implementation of industry-standard file formats is not dependent on the action of rival EDA vendors (including the Merged Entity).[679] In the second place, the Commission has found no indications of the Parties totally restricting or degrading baseline interoperability in the past.

(720) **Second**, the majority of market participants providing a view during the market investigation also confirmed that it is unlikely or even impossible that the Merged Entity would totally *remove* baseline interoperability between HFSS and third-party EDA tools.[680] Similarly, the majority of market participants providing a view

679 Parties' Paper on the Baseline Interoperability in EDA, paras 19-25.

680 Replies to Questionnaire to customers of EDA and design IP, question D.B.C.4.

during the market investigation considered that the Merged Entity would unlikely have the ability to *degrade* such interoperability.[681]

(721) On the basis of all these elements, and for the purposes of this Decision, the Commission has reached the conclusion that the Merged Entity **would unlikely have the ability** to engage in a strategy of market-wide foreclosure of competing providers of EDA tools by totally restricting or degrading interoperability between HFSS and third-party EDA tools in any of the affected interoperability pairings relating to electromagnetic simulation tools specified in Annex A of the Decision.

5.4.6.3.1.2.2. Total restriction and/or degradation of interoperability is an unlikely foreclosure strategy because interoperability is an important element of the EDA industry

(722) For the reasons explained below, the Commission considers that, even if it was possible to technically restrict or degrade interoperability between HFSS and third-party EDA tools, the Merged Entity would unlikely engage in this foreclosure mechanism to foreclose rival EDA providers.

(723) **First**, for the reasons outlined in Section 5.4.5.3.1.2.3, the Merged Entity would unlikely engage in this foreclosure mechanism against its EDA rivals because interoperability is an important element of the EDA industry in which EDA vendors are generally incentivised to maintain effective interoperability.

(724) **Second**, as described in Section 5.4.3.1.2, customers have a significant role in demanding and maintaining effective interoperability, which the Commission considers significantly limits the Merged Entity's ability to totally restrict or degrade interoperability at its own initiative.

(725) Therefore, based on the elements considered above, and for the purposes of this Decision, the Commission considers that even if it would be technically possible to degrade interoperability (by degrading proprietary interfaces), the Merged Entity would unlikely engage in this foreclosure mechanism.

5.4.6.3.1.2.3. Not a significant proportion of customers would switch to the Merged Entity's EDA tools as a result of foreclosure

(726) For the reasons outlined in Section 5.4.5.3.1.2.4, it is unlikely that a significant proportion of customers would switch their EDA tool as a result of foreclosure of those EDA tools. As a result, even if the Merged Entity could fully leverage its alleged market power with Ansys' HFSS tool in the globally affected market for electromagnetic simulation, the Merged Entity would likely still not be able to foreclose Synopsys' rivals in the EDA markets. In particular:

(727) **First**, the market investigation indicated that customers would likely not switch their EDA tool to the benefit of the Merged Entity, as a result of foreclosure.

(728) In the first place, a majority of customers that expressed a view indicated that, in response to a hypothetical scenario where Ansys' HFSS is no longer interoperable with competitors' (non-Synopsys) EDA tools and instead only interoperates with Synopsys' EDA tools, they would switch to an alternative of HFSS or even find

681 Replies to Questionnaire to customers of EDA and design IP, question D.B.C.6.

workaround solutions (rather than switch to a Synopsys EDA tool that continues to interoperate with HFSS).[682] This is true for all EDA tools that are interoperable with HFSS.[683] In addition, a majority of customers that expressed a view indicated they would do the same even when confronted with a degradation or delay of interoperability (as opposed to a removal of interoperability).[684] For instance, one customer explained that "*We will probably first find workarounds by defining own solutions, but acquire new tool with same functionality asap*."[685], another customer submitted that "[*the Merged Entity] could decide to switch to proprietary output formats that don't interoperate with other suppliers, but if they did so the design community would quickly pivot to an alternative*."[686], and another customer similarly submitted that "*If they delayed interoperability, the design community would pivot to alternatives and/or find a workaround to the interoperability issues*.".[687] As one customer observed, "*Since Ansys HFSS is used to design and simulate high-frequency electronic products, it is important that it is interoperable with the leading EDA design solutions. If it is not, alternatives would have to be sought."*[688]

(729) **Second**, as explained above at Section 5.4.5.3.1.2.4, some customers already multi-home for their EDA tools (i.e. use two EDA vendors for one type of tool), including HFSS.[689] This enables customers to circumvent the foreclosure strategies of the Merged Entity, because they already have alternatives in place.

(730) **Third,** for the reasons outlined in Section 5.4.5.3.1.2.4. customers mix-and-match their EDA tools (i.e., purchase their EDA tools from different vendors across EDA functionalities), precisely because having an integrated portfolio of EDA tools is not the only factor that is important for customers. This suggests that customers would likely not switch to the Merged Entity's EDA tools if the interoperability with third-party EDA tools was totally restricted or degraded.

(731) **Fourth**, for the reasons outlined in Section 5.4.5.3.1.2.4, historical examples of tighter integration and greater interoperability between EDA tools demonstrate that this does not necessarily lead to customers switching to those EDA tools.

(732) **Fifth**, for the reasons outlined in Section 5.4.5.3.1.2.4, EDA vendors have not generally managed to leverage their strong market position in sign-off EDA markets into other EDA markets.

(733) **Sixth**, for the reasons outlined in Section 5.4.5.3.1.2.4, limited instances of termination and/or degradation of interoperability in the past show that (despite the Parties, as well as their rivals, possessing similar or even higher levels of market power) a significant proportion of customers would likely not switch their EDA tool to the Merged Entity's benefit as a result of foreclosure.

(734) **Seventh**, for the reasons outlined in Section 5.4.5.3.1.2.4, EDA customers include very large chip design companies with significantly higher turnovers than the

682 Replies to Questionnaire to customers of EDA and design IP, question D.B.C.10.
683 That is: Circuit Simulation, Layout and Photonic Layout Design Implementation.
684 Replies to Questionnaire to customers of EDA and design IP, question D.B.C.12.
685 Replies to Questionnaire to customers of EDA and design IP, question D.B.C.13.
686 Replies to Questionnaire to customers of EDA and design IP, question D.B.C.4.
687 Replies to Questionnaire to customers of EDA and design IP, question D.B.C.7.
688 Replies to Questionnaire to customers of EDA and design IP, question D.B.C.2.1.
689 Replies to Questionnaire to customers of EDA and design IP, question D.B.C.1.

Merged Entity (e.g. Nvidia, Intel, Google, Apple), who will likely push back against any foreclosure strategy of the Merged Entity by either switching to competitors' tools or by using their bargaining power to ensure the Merged Entity did not foreclose other EDA vendors.

(735) Based on the elements considered above, and for the purposes of this Decision, the Commission has reached the conclusion that even if the Merged Entity totally restricted or degraded interoperability between HFSS and third-party EDA tools, it would unlikely have the ability to leverage Ansys' position in the worldwide market for electromagnetic simulation with HFSS to foreclose Synopsys' rivals in the EDA markets.

5.4.6.3.1.2.4. Main EDA rivals are able to deploy effective and timely counter-strategies

(736) For the reasons outlined below, the Commission considers that Synopsys' rivals in the EDA markets Cadence, Siemens and Keysight are able to deploy effective and timely counterstrategies in response to a potential foreclosure strategy of the Merged Entity of restricting or degrading interoperability between HFSS and third-party EDA tools.

(737) **First**, the Commission considers that Synopsys' main EDA rival, Cadence, is a strong EDA competitor that has its own electromagnetic simulation tool EMX ([30-40]% market share worldwide by revenue in 2023), the market share of which has been increasing from [20-30]% in 2022 to [30-40]% in 2023. Further, Cadence's market position, range of EDA tools across various functions and capabilities make it able to effectively respond to a potential foreclosure strategy. For instance, one customer submitted that in the face of a foreclosure strategy "*Other companies in the EDA space (like Cadence and Siemens) would likely continue to offer interoperable solutions. If a merged entity were to limit integration, it could lose market share to competitors who provide more open and flexible solutions*.".[690]

(738) **Second**, the Commission notes that another EDA competitor, Keysight, offers alternative tools for electromagnetic simulation (PathWave EM Design - EMPro), and has seen its worldwide market share by revenue increase from [10-20]% in 2021 to [10-20]%in 2023. The Commission has no indication that Keysight would not be able to deploy effective and timely counterstrategies, for example by combining its electromagnetic simulation tool with third-party EDA tools, in particular Siemens'.

(739) **Third**, for the reasons outlined in Section 5.4.5.3.1.2.5, the Commission considers that mutual dependence for interoperability between EDA vendors (and particularly Cadence and Siemens) gives Synopsys' rivals the possibility to retaliate against any possible foreclosure strategy by the Merged Entity.

5.4.6.3.1.3. The Merged Entity's ability to foreclose competing providers of EDA tools by engaging in anti-competitive bundling

(740) The Commission considers that the Merged Entity would not have the ability to engage in a strategy of market-wide foreclosure strategy, to foreclose competing providers of EDA tools by engaging in anti-competitive (pure and/or mixed) bundling between HFSS and third-party EDA tools, for the reasons outlined in

690 Replies to Questionnaire to customers of EDA and design IP, question D.B.A.8.1.

Section 5.4.5.3.1.3 that also apply to the Commission's assessment in the present section.

5.4.6.3.1.4. Conclusion on the Merged Entity's ability to foreclose competing providers of EDA tools by leveraging Ansys' electromagnetic simulation tool HFSS

(741) On the basis of all these elements, and for the purposes of this Decision, the Commission considers it unlikely that the Merged Entity would have the ability to engage in a strategy of market-wide foreclosure strategy, to foreclose competing providers of EDA tools by totally restricting or degrading interoperability between HFSS and third-party EDA tools in any of the affected interoperability pairings relating to Ansys' tools in electromagnetic simulation specified in Annex A of the Decision or by means of anti-competitive (pure and/or mixed) bundling between HFSS and third-party EDA tools, in any possible bundle pairings.

5.4.6.3.2. Incentive to foreclose

(742) For the reasons set out below, the Commission has reached the conclusion that the Merged Entity **would not have the incentive** to engage in a strategy of market-wide foreclosure of competing providers of EDA tools by totally restricting or degrading interoperability between HFSS and third-party EDA tools in any of the affected interoperability pairings relating to electromagnetic simulation tools specified in Annex A of the Decision, or by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings.[691]

(743) **First**, the reasons outlined in Section 5.4.5.3.2 also apply to the Commission's assessment in the present section. Further, the Commission expects the incentive to foreclose to be even less likely in the global electromagnetic simulation market, since HFSS is a broad-purpose tool, as set out above at paragraph 346, whereby chip design only accounted for about [a small percentage]% of its revenue in 2023[692] and [a small percentage]% amount to [a small percentage] of RedHawk(-SC)'s revenue as a gate-level power integrity too.[693]

(744) **Second,** not a single customer expressing a view during the market investigation indicated that, in response to the Merged Entity delaying or degrading the interoperability between HFSS and competitors' (non-Synopsys) EDA tools, it would switch to a Synopsys EDA tool that continues to interoperate with Ansys' HFSS. Customers expressing a view indicated that they would rather switch to an alternative to HFSS[694] or develop their own customised flow between HFSS and competitors' EDA tools.[695] In this event, the Merged Entity would forgo significant sales of its HFSS tool, and therefore make considerable losses from such foreclosure strategies.

(745) In light of the above, the Commission has reached the conclusion that the Merged Entity **would not have the incentive** to engage in a strategy of market-wide

691 Except for when it specifically relates to interoperability, the Commission's assessment of the Merged Entity's incentive to leverage Ansys' potentially strong market position electromagnetic simulation to foreclose EDA competitors also applies to a potential concern of anticompetitive (pure and/or mixed) bundling.

692 Form CO, para. 1088.

693 Form CO, Annex PN RFI 1 Q14.

694 Replies to Questionnaire to customers of EDA and design IP, question D.B.C.11.

695 Replies to Questionnaire to customers of EDA and design IP, question D.B.C.12.

foreclosure of competing providers of EDA tools by totally restricting or degrading interoperability between HFSS and third-party EDA tools in any of the affected interoperability pairings relating to electromagnetic simulation tools specified in Annex A of the Decision, or by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings.

5.4.6.3.3. Impact on effective competition

(746) Given that the Commission has reached the conclusion that the Merged Entity would not have the ability or incentive to engage in a strategy of market-wide foreclosure strategy by totally restricting or degrading interoperability between HFSS and third-party EDA tools in any of the affected interoperability pairings relating to electromagnetic simulation tools specified in Annex A of the Decision, or by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings, the Commission has not assessed whether the impact of such foreclosure strategies would lead to a significant impediment to effective competition.

5.4.6.3.4. Conclusion

(747) In view of the above considerations and in light of the results of the market investigation and the evidence and information available to it, the Commission concludes that the Transaction does not raise serious doubts as to its compatibility with the internal market as a result of conglomerate effects, notably by foreclosing competing providers of EDA tool through leveraging of Ansys' electromagnetic simulation tool HFSS, considering that the Merged Entity would not have the ability and incentive to engage in such strategy.

5.4.7. Leveraging from Ansys' position in other conglomerate leveraging markets to foreclose Synopsys' rivals in the EDA markets

(748) The Commission has assessed together concerns relating to Ansys' products in the eight conglomerate leveraging markets outlined in Table 42 in Section 5.4.1 where Ansys is active and that are not assessed separately in Sections 5.4.5 and 5.4.6 ("**eight other conglomerate leveraging markets**"), i.e., the worldwide markets for (i) gate-level security analysis, (ii) clock jitter analysis, (iii) parasitic analysis, (iv) power device analysis, (v) RTL power consumption analysis, (vi) transistor-level power integrity analysis, (vii) structural and thermal analysis, and (viii) signal and power integrity analysis.

(749) As outlined in Section 5.4.1, the Commission assesses these eight other conglomerate leveraging markets together, because conglomerate concerns seem less likely in these markets (compared to the markets assessed in Sections 5.4.5 and 5.4.6) in view of the concerns expressed by market participants and the market position of the Parties (and particularly Ansys) in these markets (see Section 5.4.7.3.1 below for further detail). In addition, the reasons supporting the Commission's conclusion on the Merged Entity's ability and incentive to foreclose EDA competitors by leveraging Ansys' potentially strong position apply across all eight other conglomerate leveraging markets.

5.4.7.1. Potential concern

(750) As explained in Section 5.4.5.1, the foreclosure concerns raised by the market participants primarily focused on the Merged Entity's ability and incentive to leverage Ansys' gate-level power integrity tool RedHawk(-SC) to foreclose EDA

competitors, since RedHawk(-SC) is considered the industry's "golden standard" and is Ansys' most popular product.

(751) However, these market participants also considered that the possible foreclosure strategies would also apply leveraging from any other markets for EDA tools where Ansys could potentially have market power. To address all potential concerns with respect to the leveraging of Ansys' market position in other EDA markets, the Commission has investigated whether the Merged Entity would have the ability and incentive to leverage Ansys' potentially strong position in each of the eight conglomerate leveraging markets into neighbouring EDA markets (based on both interoperability pairings and bundle pairings) where Synopsys is active, and whether such a foreclosure strategy would have a significant detrimental effect on competition in the relevant markets.

(752) As outlined in Section 5.4.3, the Commission has assessed two potential concerns, namely (i) the total restriction or degradation of interoperability between these Ansys' tools and third-party EDA tools, and (ii) anticompetitive (pure and/or mixed bundling) with these Ansys' tools and Synopsys' products. The specific foreclosure mechanisms assessed are equivalent to those outlined in Sections 5.4.5.1.

5.4.7.2. The Notifying Party's view

(753) For the same reasons as outlined in Section 5.4.4, the Notifying Party submits that the Merged Entity will lack the ability and the incentive to leverage Ansys' EDA tools to foreclose competitors in the EDA markets by degrading/removing interoperability or by means of anticompetitive bundling/tying, and that any foreclosure strategy would not significantly impede effective competition.

5.4.7.3. The Commission's assessment

5.4.7.3.1. Ability to foreclose

(754) For the reasons set out below, the Commission has reached the conclusion that the Merged Entity **would not have the ability** to engage in a strategy of market-wide foreclosure of competing providers of EDA tools by totally restricting or degrading interoperability between Ansys' tools in any of the eight other conglomerate leveraging markets and rival EDA tools in any of the relevant affected interoperability pairings specified in Annex A of the Decision, or by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings.[696]

(755) **First**, whilst the Commission cannot exclude that Ansys holds a significant degree of market power in any of the eight other conglomerate leveraging markets because of its significant market shares (see Section 5.4.1), the Commission considers that the market power of these Ansys tools is likely less than that of Ansys' RedHawk(-SC). This is because Ansys' flagship product RedHawk(-SC) is considered the industry's "golden standard" and is viewed by many market participants as particularly important.[697] The Commission has seen no evidence to

[696] Except for when it specifically relates to interoperability, the Commission's assessment of the Merged Entity's ability to leverage Ansys' potentially strong market position in the eight other conglomerate leveraging markets to foreclose EDA competitors also applies to a potential concern of anticompetitive (pure and/or mixed) bundling.

[697] See Section 5.4.5.

suggest this is true for Ansys' tools in any of the eight other conglomerate leveraging markets. This fact is reflected in Ansys' revenues, where RedHawk(-SC) alone accounts for [a significant percentage]Ansys' total EDA-related revenue.[698] By contrast, Ansys' tools in the eight other conglomerate leveraging markets together account for [a small percentage] RedHawk(-SC)'s revenue.[699] In addition, compared to the gate-level power integrity analysis market, each of the eight other conglomerate leveraging markets have a significantly smaller total market size.[700] This reflects the fact that most of these EDA tools perform an optional functionality that is less important in the chip design compared to gate-level power integrity analysis that is performed by RedHawk(-SC).

(756) **Second**, as explained further in detail in Section 5.4.7.3.1.1 the Commission considers that the Merged Entity would not have the technical ability to totally restrict or degrade interoperability between Ansys' tools in any of the eight other conglomerate leveraging markets to foreclose rival EDA providers because effective interoperability will remain possible based on industry-standard interfaces for almost all affected interoperability pairings, or customers could potentially find workaround solutions to continue using the given EDA tools.

(757) **Third**, as explained further in detail in Section 5.4.7.3.1.2 the Commission considers that the Merged Entity would not have the ability to leverage its position in any of the eight other conglomerate leveraging markets to foreclose rival EDA providers by totally restricting or degrading interoperability or by means of anticompetitive (pure and/or mixed) bundling because it is unlikely that a significant proportion of customers would switch to EDA tools, and Synopsys' main rivals in the EDA markets, Cadence and Siemens, would be able to deploy effective and timely counterstrategies in the face of any foreclosure strategy.

5.4.7.3.1.1. No technical ability to totally restrict interoperability between Ansys' EDA tools and third-party EDA tools in the eight other conglomerate leveraging markets

(758) As a preliminary point in that regard, the Commission notes that interoperability between Ansys' tools in the eight other conglomerate leveraging markets and third-party EDA tools is primarily achieved through industry-standard interfaces. As shown in Table 46 below, there are only 6 (out of 53) relevant affected interoperability pairings in which Ansys' tools interoperate with third-party (non-Synopsys) EDA tools based on proprietary interfaces. This concerns Ansys' gate-level security analysis tool (RedHawk(-SC) Security), RTL power consumption analysis tool (PowerArtist), transistor-level power integrity analysis tool (Totem), power device analysis tool (PowerX), and parasitic analysis tool (ParagonX).

(759) For the reasons explained below, whilst the Commission cannot exclude that the Merged Entity would have the technical ability to degrade interoperability based on proprietary interfaces that exist in limited instances of pairings, the Commission considers that the Merged Entity would not have the technical ability to totally restrict or degrade interoperability between Ansys' tools in the eight other

698 Form CO, paragraph 21.

699 Form CO, Annex RFI 14 Q.5 – 001 showing an overview of the functions in which Ansys' shares exceed 30% including a comparison of total market sizes and Ansys' revenues.

700 Ibid.

conglomerate leveraging markets and third-party EDA tools based on industry-standard file formats (i.e. baseline interoperability).

(760) **First**, for the reasons outlined in Section 5.4.5.3.1.2.1. a) above, the Commission concludes that the Merged Entity would unlikely have the ability to *totally restrict* interoperability between Ansys' tools in the eight other conglomerate leveraging markets and third-party EDA tools based on proprietary interfaces but cannot exclude that the Merged Entity would have the technical ability to *degrade* such interoperability. However, despite different mechanisms for degrading such interoperability described by some market participants, the Commission notes that the Merged Entity would have a limited scope to degrade interoperability between Ansys' tools in the eight other conglomerate leveraging markets and third-party EDA tools.

(761) *In particular,* in the pairing between Ansys' RedHawk(-SC) Security and third-party timing analysis tools, [details of Ansys' interoperability agreements with competitors].

(762) **Second**, for the reasons outlined in Section 5.4.5.3.1.2.1. b) above that also apply to interoperability between Ansys' tools in the eight other conglomerate leveraging markets and third-party EDA tools, the Commission considers that the Merged Entity would not have the technical ability to totally restrict or degrade interoperability between Ansys' tools and third-party EDA tools based on *industry-standard interfaces*.

(763) **Third**, the Commission considers that the Merged Entity would likely not have the technical ability to totally restrict interoperability, because effective interoperability will remain possible based on industry-standard interfaces, for almost all of the eight affected interoperability pairings.

(764) In the first place, as indicated in Table 46 below, interoperability between Ansys' tools in the eight other conglomerate leveraging markets and third-party EDA tools is predominantly based on industry-standard file formats, and there are only 6 pairings in which interoperability is based on proprietary interfaces.

(765) In the second place, as explained in Section 5.4.3, as a rule, even when interoperability between EDA tools is established through proprietary interfaces, an equivalent industry-standard file format exists as an alternative, i.e. in most cases the same EDA tools can perform the same analysis through an industry-standard file format as they do with proprietary file formats.[701]

(766) As Table 46 below shows, for 5 out of 6 affected interoperability pairings in which Ansys' EDA tools interoperate with third-party (non-Synopsys) EDA tools based on proprietary interfaces, an alternative industry standard file format exists through which interoperability can be achieved. For only 1 interoperability pairing, there is no industry-standard file format alternative. This concerns RedHawk(-SC) Security as gate-level security analysis tool for which Ansys requests Cadence's timing analysis tool (Tempus) to output in a file format that can be read by RedHawk(-SC) Security.

701 Parties' Paper on the Lack of Interoperability Concerns, para. 22.

Table 46: Alternative industry-standard file formats for interoperability between Ansys' EDA tools and third-party (non-Synopsys) EDA tools

EDA market segment **(Ansys' tool)**	**Data flow direction and function of third-party (non-Synopsys) EDA tools**	**Proprietary interface**	**Alternative industry-standard interface**
RTL power consumption analysis (PowerArtist)	[…]	[Ansys' interoperability agreements with competitors]	Yes
Transistor-level power integrity analysis (Totem(+SC))	[…]	[Ansys' interoperability agreements with competitors]	Yes
Power device analysis (PowerX)	[…]	[Ansys' interoperability agreements with competitors]	Yes
Parasitic analysis (ParagonX)	[…]	[Ansys' interoperability agreements with competitors]	Yes
Transistor-level power integrity analysis (Totem+SC)	[…]	[Ansys' interoperability agreements with competitors]	Yes
Gate-level security analysis (RedHawk-SC Security)	[…]	[Ansys' interoperability agreements with competitors]	No

(767) **Fourth**, as explained in Section 5.4.5.3.1.2.1 a) above, the results of the market investigation and the Parties' internal documents indicate that customers may find workaround solutions to solve and prevent interoperability issues. Therefore, even in exceptional instances where there is no alternative industry-standard that allows the same interoperability between respective EDA tools, customers can and do find workaround solutions to maintain interoperability.

(768) On the basis of all these elements, and for the purposes of this Decision, the Commission has reached the conclusion that even if the Merged Entity would have the technical ability to degrade interoperability based on *proprietary interfaces*, the

Merged Entity would likely **not have the technical ability to totally restrict interoperability** between Ansys' tools in the eight other conglomerate leveraging markets and third-party EDA tools, because (i) effective interoperability will remain possible based on industry-standard interfaces for almost all affected interoperability pairings involving the eight other conglomerate leveraging markets, and (ii) customers can and do find workaround solutions to solve and prevent interoperability issues.

5.4.7.3.1.2. No ability to leverage the Merged Entity's position in the eight other conglomerate leveraging markets

(769) For the reasons explained below, the Commission considers that the Merged Entity would not have the ability to leverage its position in any of the eight other conglomerate leveraging markets to foreclose rival EDA providers by totally restricting or degrading interoperability or by means of anticompetitive (pure and/or mixed) bundling.

(770) **First**, for the reasons outlined in Section 5.4.5.3.1.2.3, the Merged Entity would unlikely engage in this foreclosure mechanism to foreclose its EDA rivals because the characteristic features of demand and supply in the EDA industry generally incentivize EDA vendors to maintain effective interoperability in the EDA markets.

(771) **Second**, for the reasons outlined in Section 5.4.5.3.1.2.4., it is unlikely that a significant proportion of customers would switch their EDA tool as a result of foreclosure of rival EDA tools. In that respect, when asked, several customers were explicit about their counterstrategies (switching to rival EDA alternatives or finding workaround solutions) should they be bereft of their mixing-and-matching ability. As one customer submitted "*If the supplier degraded or removed interoperability, the design community would pivot to alternatives and/or find a workaround to the interoperability issues*."[702] As a result, even if the Merged Entity could fully leverage its alleged market power with Ansys' tools in the eight other conglomerate leveraging markets, the Merged Entity would likely still not be able to foreclose Synopsys' rivals in the markets for EDA tools.

(772) **Third**, the Commission considers that, compared to a foreclosure strategy relating to RedHawk(-SC) as a gate-level power integrity tool, it is even less likely that a significant proportion of customers would switch as a result of a foreclosure strategy relating to Ansys' tools in the eight other conglomerate leveraging markets. RedHawk(-SC) as a gate-level power integrity tool is "Ansys' strongest and most successful tool, which accounts for [a significant percentage] Ansys' EDA revenues", and is viewed by many market participants as particularly important. In contrast, Ansys' tools in the eight other conglomerate leveraging markets are […] – they together account for [a small percentage] RedHawk(SC)'s revenue.[703].[704].[705] In addition, most of these EDA tools perform an optional functionality that is less important in the chip design compared to gate-level power integrity analysis that is performed by RedHawk(-SC), which is also reflected in their significantly smaller total market sizes relative to gate-level power integrity

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702 Replies to Questionnaire to customers of EDA and design IP, question D.B.F.1.1.

703 Form CO, paragraph 21.

704 See Section 5.4.5.

705 Form CO, Annex RFI 14 Q.5 – 001 showing an overview of the functions in which Ansys' shares exceed 30% including a comparison of total market sizes and Ansys' revenues.

analysis.[706] Therefore, the Commission expects fewer customers to switch from rivals' EDA tools to Synopsys' EDA tools if the Merged Entity leveraged Ansys' tools in the eight other conglomerate leveraging markets, compared to if it leveraged RedHawk(-SC) to foreclose its competitors. This is also reflected in the fact that the concerns expressed by some market participants about potential foreclosure of EDA rivals primarily or only concerned RedHawk(-SC), and to a limited degree or not at all to other Ansys' EDA tools.

(773) **Fourth**, for the reasons outlined in Section 5.4.5.3.1.2.5, the Commission considers that Synopsys' main rivals in the EDA markets, Cadence and Siemens, are able to deploy effective and timely counterstrategies to the Merged Entity foreclosing them in any of the eight other conglomerate leveraging markets. Again, in light of the particular importance of RedHawk(-SC), the Commission expects Cadence and Siemens to be more able to deploy effective and timely counterstrategies if the Merged Entity leveraged Ansys' tools in the eight other conglomerate leveraging markets to foreclose its competitors, compared to if it leveraged RedHawk(-SC) for that purpose.

(774) **Fifth**, the majority of customers, when asked, did not express concerns that the Parties would totally restrict or degrade interoperability (industry-standard based and/or proprietary) between any Ansys or Synopsys' EDA tool(s) (other than RedHawk(-SC) and HFSS).[707] This was the case even though several (albeit a minority of) customers indicated there were some EDA tools of the Parties that had few or no alternatives, mainly Ansys' transistor-level power integrity analysis tool Totem and Synopsys' TCAD tools. Several customers indicated they do not have such concerns because they expect the interoperability to be maintained and/or ensured through industry standards, and others because they would have sufficient counterstrategies and/or alternatives to counter any foreclosure strategies. As one customer explained, "*currently, Synopsys and Ansys tools are compatible with those offered by other EDA providers, such as Cadence and Siemens. This interoperability is a key aspect of what makes these tools valuable to customers, and [the customer] expects that Synopsys will maintain this model in the future*." Adding that "*Any attempt by Synopsys to limit the compatibility of its products with those of other companies would make them less attractive to [the customer] and semiconductor design firms and would not be a commercially viable strategy*".[708] This supports the reasons outlined in this Section.

(775) **Finally**, on the basis of the elements already outlined in Section 5.4.5.3.1.3, the Commission considers that the Merged Entity would not have the ability to foreclose competing providers of EDA tools by engaging in anti-competitive (pure and/or mixed) bundling between Ansys' tools in any of the eight other conglomerate leveraging markets and Synopsys' EDA tools.

(776) In light of the above, and for the purpose of this Decision, the Commission has reached the conclusion that the Merged Entity **would not have the ability** to engage in a strategy of market-wide foreclosure of competing providers of EDA tools by totally restricting or degrading interoperability between Ansys' tools in any of the eight other conglomerate leveraging markets and rival EDA tools in any

706 Ibid.
707 Replies to Questionnaire to customers of EDA and design IP, questions D.B.F.1 and D.B.F.1.1.
708 Replies to Questionnaire to customers of EDA and design IP, question D.B.F.1.1.

of the affected interoperability pairings specified in Annex A of the Decision, or by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings.

5.4.7.3.2. Incentive to foreclose

(777) For the reasons set out below, the Commission has reached the conclusion that the Merged Entity **would not have the incentive** to engage in a strategy of market-wide foreclosure of competing providers of EDA tools by totally restricting or degrading interoperability between Ansys' tools in any of the eight other conglomerate leveraging markets and rival EDA tools in any of the affected interoperability pairings specified in Annex A of the Decision, or by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings.[709]

(778) The Commission has come to this conclusion for the reasons outlined in Section 5.4.5.3.2. Moreover, in light of the particular importance of RedHawk(-SC) as a gate-level power integrity tool relative to other EDA tools of Ansys, as outlined in Section 5.4.7.3.1, the Commission considers that, compared to a foreclosure strategy relating to RedHawk(-SC) as a gate-level power integrity tool, it is even less likely that a significant proportion of customers would switch as a result of a foreclosure strategy relating to Ansys' tools in the eight other conglomerate leveraging markets. As such, the Commission expects the incentive to foreclose to be lower if the Merged Entity leveraged Ansys' tools in the eight other conglomerate leveraging markets to foreclose its competitors, compared to if it leveraged RedHawk(-SC) for that purpose.

(779) Further, as outlined in the Section 5.4.7.1, the majority of customers were not concerned that the Parties would delay, degrade or restrict interoperability (industry-standard based and/or proprietary) between any Ansys or Synopsys' EDA tool(s) (other than RedHawk(-SC) and HFSS).[710] This was the case even though several (albeit a minority of) customers indicated there were some EDA tools of the Parties that had few or no alternatives, mainly Ansys' Totem and Synopsys' TCAD tools. Several customers indicated they do not have such concerns, because they would have sufficient counterstrategies and/or alternatives to counter any foreclosure strategies. "*We do not anticipate any significant concerns regarding interoperability delays or degradations. Should such issues occur, we are prepared to implement flexible strategies to mitigate their impact*." Another customer submitted that they are not concerned about a restriction or degradation of interoperability because "*It would not be in the interests of the Parties as it could potentially result in loss of business as customers may switch to offerings from competitors that do not have such interoperability issues*." Another customer replied that "*If the supplier degraded or removed interoperability, the design community would pivot to alternatives and/or find a workaround to the interoperability issues*."[711] This supports the reasons outlined in this Section.

(780) In light of the above, and for the purpose of this Decision, has reached the conclusion that the Merged Entity **would not have the incentive** to engage in a

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709 Except for when it specifically relates to interoperability, the Commission's assessment of the Merged Entity's ability to leverage Ansys' potentially strong market position in any of the eight other conglomerate leveraging markets to foreclose EDA competitors also applies to a potential concern of anticompetitive (pure and/or mixed) bundling.

710 Replies to Questionnaire to customers of EDA and design IP, questions D.B.F.1 and D.B.F.1.1.

711 Replies to Questionnaire to customers of EDA and design IP, question D.B.F.1.1.

strategy of market-wide foreclosure of competing providers of EDA tools by totally restricting or degrading interoperability between Ansys' tools in any of the eight other conglomerate leveraging markets and rival EDA tools in any of the affected interoperability pairings specified in Annex A of the Decision, or by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings.

5.4.7.3.3. Impact on effective competition

(781) Given that the Commission has reached the conclusion that the Merged Entity would not have the ability or incentive to engage in a strategy of market-wide foreclosure of competing providers of EDA tools by totally restricting or degrading interoperability between Ansys' tools in any of the eight other conglomerate leveraging markets and rival EDA tools in any of the affected interoperability pairings specified in Annex A of the Decision, or by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings, the Commission has not assessed whether the impact of such foreclosure strategies would lead to a significant impediment to effective competition.

(782) However, the evidence outlined in Section 5.4.5.3.3 indicates that the effect would in any case be limited.

(783) Moreover, in light of the particular importance of RedHawk(SC) as a gate-level power integrity tool, the Commission expects the impact of such foreclosure strategies to be lower if Ansys' tools in the eight other conglomerate leveraging markets were foreclosed, compared to if RedHawk(-SC) was leveraged to foreclose. This is mainly because customers would be less likely to switch to their EDA tool as a result of foreclosure and more likely to switch to an alternative of Ansys' tools in the eight other conglomerate leveraging markets.

5.4.7.3.4. Conclusion

(784) In view of the above considerations and in light of the results of the market investigation and the evidence and information available to it, the Commission concludes that the Transaction does not raise serious doubts as to its compatibility with the internal market as a result of conglomerate effects, notably by foreclosing competing providers of EDA tools through leveraging of Ansys' tools in any of the eight other conglomerate leveraging markets.

5.4.8. Leveraging from Synopsys' position in conglomerate leveraging EDA markets to foreclose Ansys' rivals in the EDA markets

(785) The Commission has assessed together concerns relating to Synopsys' products in the 27 conglomerate leveraging EDA markets outlined in Tables 42 and 43 in Section 5.4.1 above where Synopsys is active ("**Synopsys conglomerate leveraging EDA markets**").

(786) As outlined in Section 5.4.2., the Commission assesses the Synopsys conglomerate leveraging EDA markets together, because conglomerate concerns seem even less likely in these markets (compared to the markets assessed in Sections 5.4.5-5.4.7) in view of the concerns expressed by market participants (see Section 5.4.8.1. below for further detail). In addition, the reasons supporting the Commission's conclusion on the Merged Entity's ability and incentive to foreclose EDA competitors by leveraging Synopsys' potentially strong position apply across all Synopsys conglomerate leveraging markets.

5.4.8.1. Potential concern

(787) As explained in Section 5.4.5.1., the foreclosure concerns expressed by some market participants focused on the leveraging of Ansys' successful EDA tools and Ansys' position in EDA markets, namely in view of the fact that Ansys is currently viewed as "Swiss-neutral" because it offers its EDA tools on a standalone basis and maintains effective interoperability with third-party EDA tools.

(788) However, two market participants submitted that Synopsys has several strong EDA tools it could leverage to foreclose Ansys' EDA rivals. As one market participant explained, Synopsys has other "*must-have tools in particular for synthesis (e.g., Synopsys' Design Compiler for RTL Synthesis)*", which "*reduces any countervailing buyer power that customers have, in particular since Synopsys offers all these tools as part of an integrated, bundled offering*".[712]

(789) The Commission has therefore assessed a potential competition concern whereby the Merged Entity would have the ability and incentive to leverage Synopsys' potentially strong position in EDA tools, in each of the Synopsys conglomerate leveraging EDA markets into neighbouring EDA markets (based on both interoperability pairings and bundle pairings) where Ansys is active, and whether such a foreclosure strategy would have a significant detrimental effect on competition in the relevant markets.

(790) As outlined in Section 5.4.3. above, the Commission has separately assessed two potential concerns in respect of the Synopsys conglomerate leveraging EDA markets: (i) total restriction or degradation of interoperability between these Synopsys' tools and third-party EDA tools, and (ii) anticompetitive (pure and/or mixed bundling) with Ansys' tools and Synopsys' products. The specific foreclosure mechanisms assessed are equivalent to those outlined in Sections 5.4.5.1.

5.4.8.2. The Notifying Party's view

(791) For the same reasons as outlined in Section 5.4.4. above, the Notifying Party submits that the Merged Entity will lack the ability and the incentive to leverage Synopsys' EDA tools to foreclose competitors in the EDA markets by degrading/removing interoperability or by means of anticompetitive bundling/tying, and that any foreclosure strategy would not significantly impede effective competition.

5.4.8.3. The Commission's assessment

5.4.8.3.1. Ability to foreclose

(792) For the reasons set out below, the Commission has reached the conclusion that the Merged Entity **would not have the ability** to engage in a strategy of market-wide foreclosure of competing providers of EDA tools by totally restricting or degrading interoperability between Synopsys' tools in any of the Synopsys conglomerate leveraging markets and rival EDA tools in any of the affected interoperability

712 Market participant's response to the CMA's RFI of 21 October, question 5.

pairings specified in Annex A of the Decision, or by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings.[713]

(793) This conclusion holds despite the fact that, in light of the significant market shares (see Section 5.4.1.), the Commission cannot exclude that Synopsys holds a significant degree of market power in some of the Synopsys conglomerate leveraging EDA markets.

(794) For the reasons explained below, whilst the Commission cannot exclude that the Merged Entity would have the technical ability to degrade interoperability based on (limited instances of) proprietary interfaces, the Commission considers that the Merged Entity would not have the technical ability to totally restrict or degrade interoperability ensured through industry-standard file formats (i.e., baseline interoperability).

(795) **First**, for the reasons outlined in Section 5.4.5.3.1.2.1 a), the Commission concludes that the Merged Entity would unlikely have the ability to *totally restrict* interoperability between Synopsys' EDA tools and third-party EDA tools based on proprietary interfaces but cannot exclude that the Merged Entity would have the technical ability to *degrade* such interoperability.

(796) **Second**, for the reasons outlined in Section 5.4.5.3.1.2.1. b), the Commission considers that the Merged Entity would not have the technical ability to totally restrict or degrade interoperability between Synopsys' tools in Synopsys conglomerate leveraging EDA markets and third-party EDA tools based on industry-standard interfaces.

(797) **Third**, the Commission considers that the Merged Entity would likely not have the technical ability to totally restrict interoperability, because effective interoperability will remain possible based on industry-standard interfaces.

(798) In the first place, interoperability between Synopsys' EDA tools in areas where Synopsys' market share reaches or exceeds 30% worldwide by revenue in 2023 is primarily achieved through industry-standard interfaces and to a limited extent through proprietary interfaces. Synopsys identified 3 interoperability pairings involving a Synopsys conglomerate leveraging EDA market where the relevant tools interoperate based on proprietary interfaces.[714]

(799) In the second place, as explained in Section 5.4.3. as a rule, even when interoperability between EDA tools is established through proprietary interfaces, an equivalent industry-standard file format exists as an alternative. For all 3

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[713] Except for when it specifically relates to interoperability, the Commission's assessment of the Merged Entity's ability to leverage Synopsys' potentially strong market position in Synopsys conglomerate leveraging EDA markets to foreclose EDA competitors also applies to a potential concern of anticompetitive (pure and/or mixed) bundling.

[714] Parties' response to the European Commission's RFI 26, Table 2. Synopsys also identified 5 relevant instances where Synopsys grants a license to its proprietary interface FSDB APIs to Ansys' rivals. This list covers instances where Synopsys licenses FSDB to Ansys' rivals for analyses relevant for Ansys' tools (i.e., functions where Ansys is active (e.g., Gate-level Power Integrity Analysis, RTL Power Consumption Analysis) or markets that frequently neighbour functions where Ansys is active (e.g., Circuit Simulation, Place & Route)). In these cases, the use of FSDB is not limited to a specific pairing. The tools in question can (as applicable) read FSDB from or write FSDB for any other tool/function that supports FSDB. As such, there is no applicable Synopsys tool / interoperability pairing associated with these cases.

interoperability pairings involving a Synopsys conglomerate leveraging EDA market where the relevant tools interoperate based on proprietary interfaces, there is an industry standard file format that can be used as an alternative to the existing proprietary interface.

Table 47: Interoperability between Synopsys' EDA tool in market segments where Synopsys' share reaches or exceeds 30% worldwide by revenue in 2023 and third-party (non-Synopsys) EDA tools

***EDA market segment* / Synopsys' EDA tool**	***EDA market segment* / third-party EDA tool**	**Interoperability format**	**Alternative industry-standard interface**
Power Device Analysis Power (Synopsys' Device Workbench)	*Layout* (Cadence's Virtuoso Layout Editor, Siemens' Taner)	Proprietary file formats / industry standards	Yes
	Parasitic Extraction (Cadence's Quantus)	Proprietary file formats / industry standards	Yes
Timing analysis (Synopsys' PrimeTime)	*Gate-level Power Integrity Analysis* (Siemens' mPower)	Proprietary file formats / industry standards	Yes

(800) **Fourth**, the Commission considers that the Merged Entity would not have the ability to leverage its position in any of the Synopsys conglomerate leveraging EDA markets to foreclose rival EDA providers.

(801) In the first place, for the reasons outlined in Section 5.4.5.3.1.2.3., the Merged Entity would unlikely engage in this foreclosure mechanism to foreclose its EDA rivals because interoperability is an important element of the EDA industry in which EDA vendors are generally incentivised to maintain effective interoperability.

(802) In the second place, for the reasons outlined in Section 5.4.5.3.1.2.4., it is unlikely that a significant proportion of customers would switch their EDA tool as a result of foreclosure of those EDA tools. As a result, even if the Merged Entity could fully leverage its alleged market power with Synopsys' tools in the Synopsys conglomerate leveraging EDA markets, the Merged Entity would likely still not be able to foreclose Ansys' rivals in the EDA markets.

(803) In the third place, the Commission considers that there are no or very limited instances of Synopsys historically totally restricting and/or degrading interoperability between its own products and third-party EDA tools, despite Synopsys being active in 24 functions where its share reaches or exceeds 30%.[715] Based on the results of the market investigation, majority of the customers that

[715] See Tables 42 and 43 in Section 5.4.1.

expressed a view confirmed that neither Synopsys nor Ansys ever terminated/denied, degraded the quality and/or delayed interoperability between their own EDA tools and the EDA tools of rivals (in order to convince the customer to switch to the Parties' competing EDA tools).[716] Overall two market participants submitted that interoperability was restricted following Synopsys' acquisition of Dorado and its EDA tool called Tweaker in 2020, which Synopsys subsequently de-emphasised and integrated in a succeeding product PrimeClosure. However, as explained in Section 5.4.5.3.2., the Commission notes that there were no requests to purchase Tweaker from new customers while approx. [a significant percentage]% of existing Tweaker customers have chosen to migrate to PrimeClosure, and that Synopsys has been solving interoperability issues related to PrimeClosure on an ongoing basis.

(804) **Fifth**, for the reasons outlined in Section 5.4.5.3.1.2.5., the Commission considers that Synopsys' main rivals in the EDA markets, Cadence and Siemens, are able to deploy effective and timely counterstrategies to the Merged Entity foreclosing them in any of the Synopsys conglomerate leveraging EDA markets. Again, in light of the fact that the concerns expressed by some market participants primarily related to leveraging of Ansys' potentially strong market position (and notably RedHawk(-SC)) to foreclose Synopsys' EDA rivals, the Commission expects EDA rivals to have even more effective and timely counterstrategies if Synopsys' tools in the Synopsys conglomerate leveraging EDA markets were leveraged, compared to if Ansys' RedHawk(-SC) was leveraged.

(805) **Sixth**, the Commission notes that no or very limited concerns about the potential conglomerate effects of the Transaction were raised by customers and competitors with respect to leveraging Synopsys' EDA tools to foreclose Ansys' EDA competitors. The limited concerns put forward in that respect primarily related to Ansys' EDA tools, which are currently perceived as "Swiss-neutral" (i.e. interoperating with third-party EDA tools based on open interfaces), and which could change post-Transaction such that Ansys' EDA tools would no longer seamlessly interoperate with third-party EDA tools. In fact, when asked, the majority of customers, were not concerned that the Parties would delay, degrade or restrict interoperability (industry-standard based and/or proprietary) between Synopsys' EDA tool(s) and third-party EDA tools.[717] This was the case, even though several (albeit a minority of) customers indicated there were some EDA tools of Synopsys that had few or no alternatives, mainly Synopsys' TCAD tools. Several customers indicated they do not have such concerns, because interoperability would be maintained and/or ensured through industry standards, and others because they would have sufficient counterstrategies and/or alternatives to counter any foreclosure strategies. For instance, one customer considered that a potential foreclosure strategy would not be "*in the interests of the Parties as it could potentially result in loss of business as customers may switch to offerings from competitors that do not have such interoperability issues.*"[718] Another customer submitted that in response to the foreclosure strategy, they would "*implement flexible strategies to mitigate their impact*".[719] This supports the reasons outlined in this Section.

716 Replies to Questionnaire to customers of EDA and design IP, question C.B.3 and C.B.3.1.
717 Replies to Questionnaire to customers of EDA and design IP, questions D.B.F.1 and D.B.F.1.1.
718 Replies to Questionnaire to customers of EDA and design IP, question D.B.F.1.1.
719 Replies to Questionnaire to customers of EDA and design IP, question D.B.F.1.1.

(806) In light of the above, and for the purposes of this Decision, the Commission has reached the conclusion that the Merged Entity **would not have the ability** to engage in a strategy of market-wide foreclosure of competing providers of EDA tools by means of totally restricting or degrading interoperability between Synopsys' tools in any of the Synopsys conglomerate leveraging markets and rival EDA tools in any of the affected interoperability pairings specified in Annex A of the Decision, or by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings.

5.4.8.3.2. Incentive to foreclose

(807) For the reasons set out below, the Commission has reached the conclusion that the Merged Entity **would not have the incentive** to engage in a strategy of market-wide foreclosure of competing providers of EDA tools by means of totally restricting or degrading interoperability between Synopsys' tools in any of the Synopsys conglomerate leveraging markets and rival EDA tools in any of the affected interoperability pairings specified in Annex A of the Decision, or by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings.[720]

(808) **First**, the reasons outlined in Section 5.4.5.3.2 also apply to the Commission's assessment in the present section.

(809) **Second**, the Commission notes that Synopsys already maintains interoperability between its leading EDA tools and its competitors' tools, even in cases where Synopsys' EDA tools compete with said competitors' tools. For instance, Synopsys' timing analysis tool PrimeTime ([80-90]% worldwide by revenue in 2023) interoperates with Siemens' simulation verification tool Questa based on baseline interoperability, despite competition between Synopsys ([30-40]% worldwide by revenue in 2023) and Siemens ([20-30]% worldwide by revenue in 2023) in simulation verification in digital chip design. In addition, Synopsys licenses its own proprietary APIs to Siemens in simulation verification such that Siemens' Questa tool can read and write the same input as Synopsys' simulation verification tool.[721] Further, Synopsys' debug verification tool Verdi ([70-80]% worldwide by revenue in 2023), interoperates with Cadence's simulation verification tool Xcelium, despite competition between Synopsys ([30-40]% worldwide by revenue in 2023) and Cadence ([30-40]% worldwide by revenue in 2023) in simulation verification. Similarly, RTL synthesis capabilities of Synopsys' Fusion Compiler ([60-70]% worldwide by revenue in 2023), interoperate with Siemens' design-for-test tool, despite competition between Synopsys ([30-40]% worldwide by revenue in 2023) and Siemens ([10-20]% worldwide by revenue in 2023) in design-for-test tools. This principle is also applicable to Synopsys' competitors.[722] For example, Siemens' physical verification tool Calibre ([60-70]% worldwide by revenue in 2023) continues to support industry standards and Siemens provides additional support through its interoperability agreements with Synopsys.[723]

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720 Except for when it specifically relates to interoperability, the Commission's assessment of the Merged Entity's ability to leverage Ansys' potentially strong market position in any of the eight other conglomerate leveraging markets to foreclose EDA competitors also applies to a potential concern of anticompetitive (pure and/or mixed) bundling.

721 Parties' response to the European Commission's RFI 14, para. 5.5.

722 Parties' response to the European Commission's RFI 22, Table 3.

723 Parties' response to the European Commission's RFI 14, para. 5.6.

(810) **Third**, the Commission found no or very limited instances of Synopsys historically totally restricting and/or degrading interoperability between its own products and third-party EDA tools, despite Synopsys being active in 24 functions where its individual share reaches or exceeds 30% worldwide by revenue in 2023.[724] In light of that fact, the Commission considers that the Merged Entity would have little incentive to adopt such a strategy after acquiring Ansys.

(811) **Fourth**, the Commission notes that there were no or very limited concerns about the potential conglomerate effects of the Transaction with respect to leveraging Synopsys' EDA tools to foreclose Ansys' EDA competitors. The limited concerns put forward in that respect primarily related to Ansys' EDA tools.

(812) When asked, the majority of customers, were not concerned that the Parties would delay, degrade or restrict interoperability (industry-standard based and/or proprietary) between Synopsys' EDA tool(s) and third-party EDA tools.[725] This was the case, even though several (albeit a minority of) customers indicated there were some EDA tools of Synopsys that had few or no alternatives, mainly Synopsys' TCAD tools. Several customers indicated they do not have such concerns, because they would have sufficient counterstrategies and/or alternatives to counter any foreclosure strategies. "*We do not anticipate any significant concerns regarding interoperability delays or degradations. Should such issues occur, we are prepared to implement flexible strategies to mitigate their impact*." Another customer submitted that they are not concerned about a restriction or degradation of interoperability because "*It would not be in the interests of the Parties as it could potentially result in loss of business as customers may switch to offerings from competitors that do not have such interoperability issues*." Another customer replied that "*If the supplier degraded or removed interoperability, the design community would pivot to alternatives and/or find a workaround to the interoperability issues*."[726] This supports the reasons outlined in this Section.

(813) In light of the above, and for the purposes of this Decision, the Commission has reached the conclusion that the Merged Entity **would not have the incentive** to engage in a strategy of market-wide foreclosure of competing providers of EDA tools by means of totally restricting or degrading interoperability between Synopsys' tools in any of the Synopsys conglomerate leveraging markets and rival EDA tools in any of the affected interoperability pairings specified in Annex A of the Decision, or by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings.

5.4.8.3.3. Impact on effective competition

(814) Given that the Commission has reached the conclusion that the Merged Entity would not have the ability or incentive to engage in a strategy of market-wide foreclosure of competing providers of EDA tools by means of totally restricting or degrading interoperability between Synopsys' tools in any of the Synopsys conglomerate leveraging markets and rival EDA tools in any of the affected interoperability pairings specified in Annex A of the Decision, or by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings, the

724 See Tables 42 and 43 in Section 5.4.1.
725 Replies to Questionnaire to customers of EDA and design IP, questions D.B.F.1 and D.B.F.1.1.
726 Replies to Questionnaire to customers of EDA and design IP, question D.B.F.1.1.

Commission has not assessed whether the impact of such foreclosure strategies would lead to a significant impediment to effective competition.

5.4.8.3.4. Conclusion

(815) In view of the above considerations and in light of the results of the market investigation and the evidence and information available to it, the Commission concludes that the Transaction does not raise serious doubts as to its compatibility with the internal market as a result of conglomerate effects, notably by foreclosing competing providers of EDA tools through leveraging of Synopsys' EDA tools in any of the Synopsys conglomerate leveraging markets, considering that the Merged Entity would not have the ability and incentive to engage in such strategy.

5.4.9. Leveraging from Synopsys' positions in the conglomerate leveraging design IP markets to foreclose Ansys' rivals in the EDA markets

(816) Design IP and EDA are considered to belong to neighbouring markets for the following two reasons. First, companies designing a chip need to develop or procure both design IP products and EDA tools. Second, EDA tools are also used by design IP licensors to develop their design IP products.

(817) As set out above at Section 5.2.4, Synopsys individually holds a market share of more than 30% worldwide by revenue in 2023 in the plausible markets for embedded memories, physical libraries and wired interface IP (hereafter together referred to as 'conglomerate leveraging design IP markets').

(818) In all other plausible design IP markets, the market shares estimates provided by the Notifying Party are low and, in any event, significantly lower than 30%, as confirmed by the 2021-2023 market share estimates in the third-party IPnest reports submitted by the Notifying Party.[727]

(819) As mentioned above at Section 5.4.1., there are 10 interoperability pairings with EDA tools in each of the conglomerate leveraging embedded memories and physical libraries markets, and 6 interoperability pairings in the conglomerate leveraging wired interface IP market. More specifically, Synopsys' design IP products in each of these markets export data to EDA tools that are being used for clock jitter analysis, ESD analysis, early power integrity analysis, electromagnetic device synthesis, electromagnetic extraction, electromagnetic modelling, gate-level power integrity analysis gate-level security analysis, parasitic analysis, power device analysis, signal and power integrity, structural and thermal analysis, and transistor-level power integrity analysis. Design IP products in these categories do not import data from EDA tools.[728]

5.4.9.1. Potential concern

(820) The Commission has assessed a potential competition concern whereby the Merged Entity would leverage Synopsys' potentially strong position in the conglomerate leveraging design IP markets into the EDA markets where Ansys is active and thereby foreclose competitors on these markets, thus causing harm to customers.

727 Form CO, annexes PN RFI 13 Q.5 – 001-002.

728 Parties' response to the European Commission's RFI 24, Annex Q 2.1.

(821) Few market participants expressed concerns that the Merged Entity may (i) restrict or degrade interoperability between Synopsys' design IP and third-party EDA tools and/or (ii) engage in anticompetitive (pure and/or mixed bundling) between Synopsys' design IP and the Merged Entity's EDA tools.[729]

5.4.9.2. The Notifying Party's view

(822) The Notifying Party submits, first, that it would not have the ability or incentive to harm Ansys' rivals by degrading the interoperability of Synopsys' soft IP (e.g., the controller part of its wired interface IP) given that Ansys does not currently offer any of the EDA tools (e.g., RTL synthesis, design-for-test / test IP, place & route, timing Analysis) that are typically used for hardening soft IP.[730]

(823) Second, the Notifying Party submits that it would not have the ability to selectively degrade the interoperability between Synopsys' hard IP and Ansys' rival verification and sign-off tools because hard IP is based on industry-standard formats (mainly GDSII but also .lib, LEF/DEF, and Verilog) open to all EDA tools and supported by nearly all EDA tools, including Ansys' rivals. It explains that once a design has been verified through simulation to meet all specified criteria, it is sent to the foundry for tape-out in GDSII format, and that a chip design that does not support GDSII cannot be manufactured by the foundry. Therefore, the Merged Entity could not selectively degrade the interoperability of Synopsys' hard IP with Ansys' rival verification and sign-off tools without affecting the interoperability of the hard IP with other EDA and S&A tools that use these industry standards.[731]

(824) Third, the Notifying Party submits that it would lack the incentive to degrade the interoperability between Synopsys' hard IP and Ansys' rival verification and sign-off tools, for the following reasons. In the first place, in the absence of selective degradation, any attempt to degrade the interoperability of Synopsys' hard IP with rival verification and sign-off tools (i.e., by moving away from GDSII), would reduce the value of Synopsys' hard IP in the eyes of customers and would result in lost sales. In the second place, customers would reject any attempt by the Parties to depart from the industry standard formats (including through any degradation that impacts said formats) by switching to alternative providers that support the industry standard formats or developing their own workarounds. In the third place, the Parties' tools would be far less attractive to customers in the long term if they were known not to operate well with all existing best-of-breed solutions, putting future sales at risk. In the fourth place, Cadence is active in both design IP (including, among others, wired interface IP), EDA and S&A tools and could respond to any post-Transaction attempts by the Merged Entity to use Synopsys Design IP tools to foreclose Cadence in EDA markets by replicating any attempt at interoperability degradation (i.e., by degrading the interoperability of the Cadence design IP with Synopsys' EDA tools).[732]

(825) Fourth, the Notifying Party submits that the contracting processes for design IP products and for EDA tools are fundamentally separate and different, in particular

729 Market participant's response to the CMA's Questionnaire of 23 September 2024, question 9 and agreed minutes of the conference call of 1 July 2024 with a market participant.
730 Form CO, Appendix 1, Intellectual property business, para. 45.
731 Response to the European Commission's requests for information dated 22 November 2024, question 2 and dated 3 December 2024, questions 30 and 31.
732 Response to the European Commission's RFI 25, question 30.

with respect to the scope of contracts, the sales cycles and negotiation process, the teams involved in the negotiation both at Synopsys and at the customers, and the pricing structure. These differences would preclude any ability to bundle design IP products and EDA tools.[733]

5.4.9.3. The Commission's assessment

5.4.9.3.1. Ability to foreclose

(826) For the reasons set out below, the Commission has reached the conclusion that the Merged Entity **would likely not have the ability** to engage in a strategy of market-wide foreclosure of competing providers of EDA tools by totally restricting or degrading interoperability between Synopsys' products in the conglomerate leveraging design IP markets and rival EDA tools in any of the relevant affected interoperability pairings specified in Annex A of the Decision, or by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings.

(827) **First**, the Commission considers it unlikely that Synopsys holds a significant degree of market power in any of the conglomerate leveraging design IP markets (Section 5.4.9.3.1.1). **Second**, the Commission considers that the Merged Entity would likely not have the ability to foreclose competing providers of EDA tools by totally restricting or degrading interoperability between Synopsys' products in any of the conglomerate leveraging design IP markets and third-party EDA tools (Section 5.4.9.3.1.2). **Third**, the Commission considers that the Merged Entity would likely not have the ability to foreclose competing providers of EDA tools by engaging in anti-competitive (pure and/or mixed) bundling between Synopsys' products in any of the conglomerate leveraging design IP markets and the Merged Entity's EDA tools in any bundle pairings (Section 5.4.9.3.1.3)

5.4.9.3.1.1. Assessment of Synopsys' potential market power in any of the conglomerate leveraging design IP markets

(828) For the reasons explained below, as regards Synopsys' potential market power in any of the conglomerate leveraging design IP markets, **the Commission cannot exclude that Synopsys has a sufficient degree of market power** in any of these markets. This is because, on the one hand, Synopsys holds significant market shares in each of these plausible markets, and in particular in respect of embedded memories and wired interface IP. but, on the other hand, the market investigation showed that there are sufficient credible alternatives in each of said markets.

(829) **First**, the Commission notes that Synopsys holds significant market shares in respect of embedded memories, physical libraries and wired interface IP, with market shares of respectively [50-60]%,[30-40]% and [60-70]%. Other providers of embedded memories are Arm ([20-30]%), M31 ([0-10]%) and smaller competitors that account for [20-30]% of the market. For physical libraries, other providers are Arm ([30-40]%), VeriSilicon ([0-10]%), Aragio ([0-10]%) and smaller competitors that account for [20-30]% of the market. As regards wired interface IP, other competitors include Cadence ([10-20]%), AlphaWave ([0-10]%), Rambus ([0-10]%) as well as smaller competitors that account for [10-20]% of the market.[734]

733 Form CO, paragraphs 37-38 and Appendix 1, Intellectual property business, paras. 46-47.

734 Form CO, Appendix 1, Intellectual property business, paras. 34-36.

(830) **Second**, however, the customers procuring embedded memories, physical libraries and/or wired interface IP that have provided a view during the market investigation as to whether there are competitors offering products that are comparable (in terms of quality and use) to those offered by Synopsys in each of these plausible markets have responded in the affirmative.[735]

(831) As regards more specifically embedded memories, a customer noted that "*the main competitor to Synopsys is Cadence*." A second customer stated that "*Competitors include Cadence, ARM, Dolphin, Siemens EDA, M31, Silvaco, as well as the specific foundries."*. A third customer explained that it considers Cadence, M31, AlphaWave and Rambus to offer embedded memories solutions that are comparable to Synopsys'. A fourth customer mentioned Marvell, Broadcom and TSMC as having comparable offerings to Synopsys'.[736]

(832) As regards physical libraries, a customer noted that "*the main competitor to Synopsys is (...) Arm*". A second customer stated that "*Companies like Cadence and Intel offer physical libraries that can compete with those from Synopsys*." A third customer mentioned Marvell, Broadcom and TSMC. Further, several customers indicated that "*Physical libraries [may be obtained from] the foundries", with another customer specifying that "(...) foundries and foundry partners typically have comparable offerings*".[737]

(833) As regards wired interface IP, a customer noted that "(*t)here is a lot of competitions [for] wired IP*". A second customer noted that "*the main competitor to Synopsys is Cadence*". A third customer stated that "*Cadence is one of the most credible alternatives for wired interface IP*". A fourth customer explained that "*Competitors like Cadence, ARM, and Rambus provide comparable wired interface IP solutions*" A fifth customer noted that "*Competitors include companies like Cadence, Silicon Creations, Aragio"*[738].

(834) On the basis of all these elements, and for the purposes of this Decision, the Commission cannot exclude that Ansys has a significant degree of market power in any of the conglomerate leveraging design IP markets.

5.4.9.3.1.2. Ability to foreclose competing providers of EDA tools by totally restricting or degrading interoperability between Synopsys' products in the conglomerate leveraging design IP markets and third-party EDA tools

(835) For the reasons explained below, the Commission considers that the Merged Entity **would likely not have the ability** to foreclose competing providers of EDA tools by totally restricting or degrading interoperability between Synopsys' products in any of the conglomerate leveraging design IP markets and rival EDA tools in any of the relevant affected interoperability pairings specified in Annex A of the Decision.

(836) **First**, as explained by the Notifying Party, design IP products, including embedded memories, physical libraries and/or wired interface IP, interact using industry-standard formats. This is also confirmed by the market investigation, with one

735 Replies to Questionnaire to customers of EDA and design IP, question D.B.E.2.
736 Replies to Questionnaire to competitors in EDA and design IP, question D.B.E.2.1.
737 Replies to Questionnaire to competitors in EDA and design IP, question D.B.E.2.1.
738 Replies to Questionnaire to competitors in EDA and design IP, question D.B.E.2.1.

respondent stating that: "*Design IP would be based upon industry standards supported by the foundry*."[739]These industry standards are supported by nearly all EDA tools.[740] The Commission has already considered that the existence of widely used industry standards leaves little room for any selective degradation of interoperability.[741]

(837) **Second**, the majority of EDA and design IP competitors that provided a view during the market investigation have not claimed that Synopsys would have the ability to degrade the interoperability of its embedded memories, physical libraries, wired interface IP or other design IP products with competitors' EDA tools.[742]

(838) **Third**, no customer or competitor that responded to the market investigation made any mention of any removal or degradation of interoperability between Synopsys' design IP products and EDA tools in the past.

(839) Therefore, the Commission concludes that it is unlikely that the Merged Entity would have the ability to (selectively) restrict or degrade the interoperability of its design IP products in any of the relevant affected interoperability pairings specified in Annex A of the Decision with third-party EDA tools.

(840) On the basis of all these elements, and for the purposes of this Decision, the Commission has reached the conclusion that the Merged Entity **would likely not have the ability** to foreclose competing providers of EDA tools in any of the relevant affected interoperability pairings specified in Annex A of the Decision by totally restricting or degrading interoperability between Synopsys' products in any of the conglomerate leveraging design IP markets and rival EDA tools.

5.4.9.3.1.3. Ability to foreclose competing providers of EDA tools by engaging in anti-competitive bundling

(841) For the reasons explained below, the Commission considers it unlikely that the Merged Entity would have the ability to foreclose competing providers of EDA tools by engaging in anti-competitive (pure and/or mixed) bundling between Synopsys' products in any of the conglomerate leveraging design IP markets and the Merged Entity's EDA tools in any bundling pairings.

(842) **First**, as explained by the Notifying Party and confirmed by the customers that have provided a view in the market investigation, design IP products and EDA tools are generally not purchased at the same time, by the same team at the customer, from the same sales team, or under the same contract[743]. These factors would preclude any ability to engage in pure and/or mixed bundling.

(843) **Second**, the majority of customers procuring embedded memories, physical libraries and/or wired interface IP products that have provided a view in the market

739 Replies to Questionnaire to competitors in EDA and design IP, question D.B.E.4.1.

740 Response to the European Commission's RFI 24, question 2.

741 See NVIDIA/Mellanox, Case COMP/M.9424, Commission decision of 19 December 2019, paras. 209 and 221- 223.

742 Replies to Questionnaire to competitors in EDA and design IP, question D.B.E.4.

743 Form CO, paras. 37-38 and Appendix 1, Intellectual property business, paras. 46-47; replies to Questionnaire to customers of EDA and design IP, question D.B.E.3.1.

investigation indicated that Synopsys has never made the purchase of design IP products conditional upon the purchase of EDA tools.[744]

(844) **Third**, the majority of customers that have provided a view during the market investigation indicated that Synopsys has never offered them a better price or better contractual terms for buying design IP products and EDA tools from it.[745] In this respect, it must be recalled that, as explained at paragraphs 240 and 580 above, it is expensive and time-consuming for customers to switch EDA tools, which makes it unlikely that they would abandon the EDA sign-off tools they are currently using, even if the Merged Entity were to bundle design IP products and EDA tools. This is discussed in more detail in Section 5.4.10.3. below.

(845) Therefore, the Commission concludes that it is unlikely that the Merged Entity would have the ability to engage in a strategy of market-wide foreclosure of competing providers of EDA tools by engaging in anti-competitive bundling between its products in any of the conglomerate leveraging markets and its EDA tools in any bundle pairings.

5.4.9.3.1.4. Conclusion on the Merged Entity's ability to foreclose competing providers of EDA tools by leveraging its products in the conglomerate leveraging design IP markets

(846) On the basis of all these elements, and for the purposes of this Decision, the Commission has reached the conclusion that the Merged Entity **would likely not have the ability** to engage in a strategy of market-wide foreclosure of competing providers of EDA tools by totally restricting or degrading interoperability between its products in any of the conglomerate leveraging design IP markets in any of the relevant affected interoperability pairings specified in Annex A of the Decision, or by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings.

5.4.9.3.2. Incentive to foreclose

(847) For the reasons set out below, the Commission has reached the conclusion that the Merged Entity **would not have the incentive** to engage in a strategy of market-wide foreclosure of competing providers of EDA tools by totally restricting or degrading interoperability between Synopsys' products in any of the conglomerate leveraging design IP markets and rival EDA tools in any of the relevant affected interoperability pairings specified in Annex A of the Decision, or by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings.

(848) **First**, the market investigation did not provide any indication of Synopsys ever totally restricting or degrading interoperability between its design IP products and its EDA tools. This suggests that the Merged Entity would similarly not have the incentive to engage in such strategies post-Transaction.

(849) **Second**, recent evidence submitted by the Parties indicates that customers sometimes request design IP licensors and EDA vendors to enter into agreements to improve the interoperability between the providers' respective tools, for example to test and debug the connection between the design IP tool and the EDA tool in

744 Replies to Questionnaire to customers of EDA and design IP, question D.B.E.4.
745 Replies to Questionnaire to customers of EDA and design IP, question D.B.E.5.

question, and that Synopsys accedes to these requests.[746] Therefore, the Commission considers it likely that customers would oppose any removal or degradation of interoperability of Synopsys' embedded memories, physical libraries and/or wired interface IP products with EDA tools of providers other than the Merged Entity.

(850) **Third,** when asked during the market investigation how they would react if Synopsys' design IP products were available only as a bundle together with Synopsys' and Ansys' EDA tools rather than on a standalone basis, significantly more customers indicated that they would switch to design IP and EDA tools from other suppliers than those which responded that they would take the combined offering.[747]

(851) **Fourth,** whilst customers provided mixed views on how they would react if Synopsys' design IP products were available more cheaply as a bundle together with Synopsys' and Ansys' EDA tools (rather than on a standalone basis), with a small number of respondents indicating that they would take the combined offering[748], even those respondents specified that this would depend on the situation, including the quality/features of the products involved and the specifics of the offer.

(852) On the basis of all these elements, and for the purposes of this Decision, the Commission has reached the conclusion that the Merged Entity **would not have the incentive** to engage in a strategy of market-wide foreclosure of competing providers of EDA tools by totally restricting or degrading interoperability between Synopsys' products in any of the conglomerate leveraging design IP markets and rival EDA tools in any of the relevant affected interoperability pairings specified in Annex A of the Decision, or by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings.

5.4.9.3.3. Impact on effective competition

(853) Given that the Commission has reached the conclusion that the Merged Entity would not have the ability or incentive to engage in a strategy of market-wide foreclosure of competing providers of EDA tools by totally restricting or degrading interoperability between Synopsys' embedded memories, physical libraries and/or wired interface IP and rival EDA tools in any of the relevant affected interoperability pairings specified in Annex A of the Decision, or by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings, the Commission has not assessed whether the impact of such foreclosure strategies would lead to a significant impediment to effective competition.

5.4.9.3.4. Conclusion

(854) In view of the above considerations and in light of the results of the market investigation and the evidence and information available to it, the Commission concludes that the Transaction does not raise serious doubts as to its compatibility with the internal market as a result of conglomerate effects, notably by foreclosing competing providers of EDA tools through leveraging of its products in any of the

746 Form CO, Annexes PN RFI 13 Q.12-001 and 002, and Annex PN RFI 22 Q. 14.007.
747 Replies to Questionnaire to customers of EDA and design IP, question D.B.E.6.
748 Replies to Questionnaire to customers of EDA and design IP, question D.B.E.7.

conglomerate leveraging design IP markets, considering that the Merged Entity would not have the ability and incentive to engage in such strategy.

5.4.10. Leveraging from Ansys' position in conglomerate leveraging EDA markets to foreclose Synopsys' rivals in the design IP markets

5.4.10.1. Potential concern

(855) The Commission has assessed a potential competition concern whereby the Merged Entity would leverage Ansys' position in conglomerate leveraging EDA markets into one or more design IP markets where Synopsis is active and thereby foreclose competitors on these markets, thus causing harm to customers.

(856) As an initial point, the Commission notes that no market participant specifically raised concerns about Ansys leveraging its position in EDA markets to foreclose Synopsys' rivals in design IP markets. However, it must be recalled that, as mentioned above at Section 5.4.9.1., a few market participants raised concerns about the Merged Entity's ability and incentive to engage in anticompetitive bundling between its design IP products and EDA tools. Further and for the sake of completeness, it seems relevant to also address the issue of interoperability between Ansys' EDA tools and third-party design IP products, as well as the lack of necessity for third-party design IP licensors to procure EDA tools from Ansys, despite Ansys' not insignificant sales of EDA tools to Synopsys and third-party design IP licensors.[749]

(857) The Commission has separately assessed two potential concerns (i) the total restriction or degradation of interoperability between Ansys' EDA tools and third-party design IP products, and (ii) anticompetitive (pure and/or mixed) bundling between Ansys' EDA tools and Synopsys' design IP products. The specific foreclosure mechanisms assessed are equivalent to those outlined in Section 5.4.5.1.

5.4.10.2. The Notifying Party's view

(858) First, the Notifying Party submits that it would not have the ability to harm rival design IP licensors by (i) hindering their access to the Ansys S&A tools used in the development of design IP or (ii) degrading the interoperability of Ansys' S&A tools (and specifically physical verification & sign off tools) with rivals' hard IP, for the following reasons. In the first place, Ansys' S&A tools are not an important input for design IP licensors as their purchase only accounts for a small portion of their overall costs for the development of design IP. In the second place, there are several alternatives to Ansys' S&A tools. In the third place, post-Transaction, Synopsys would not have the ability to selectively degrade the interoperability of Ansys' S&A tools with Synopsys' rivals' hard IP since the latter is based on industry standard formats (in particular GDSII) that are open to all EDA and S&A tools and are supported by nearly all EDA and S&A tools.[750]

(859) Second, the Notifying Party states that it has no incentive to degrade interoperability. In the first place, in the absence of selective degradation, any attempt to degrade the interoperability of Ansys' S&A tools with rivals' hard IP

749 Form CO, Annex PN RFI 22 Q.23-001.

750 Form CO, Appendix 1, Intellectual property business, para. 43.

(i.e., by moving away from GDSII), would impact the value of Ansys' S&A tools in the eyes of customers and would result in lost sales. More specifically, the Notifying Party submits that the Parties supply large and sophisticated customers who mix-and-match the best design IP, EDA, and S&A tools for their specific requirements on a particular project ("best of breed" strategy), and therefore require suppliers' tools to interoperate. These customers would reject any attempt by the Parties to depart from this status quo (including through any degradation that impacts the industry standard hard format) by switching to alternative providers that support the industry standard format or developing their own workarounds.[751] In the second place, any attempt at foreclosure would frustrate Synopsys' design IP competitors, who could retaliate and harm Synopsys. The Notifying Party illustrates this with two examples. Firstly, it submits that Arm is the leading processor IP licensor and that it has entered into partnerships with at least six EDA and S&A tool suppliers, including Cadence, Siemens, and Synopsys to allow EDA and S&A tool suppliers to ensure that their EDA and S&A tools achieve the best possible performance metrics for Arm's processor IP and to participate in Arm-validated interoperability testing of their EDA and S&A tools with Arm's processor IP. When faced with foreclosure or any other attempt that could impact its business (including any putative attempts to foreclose competition across other design IP areas), Arm could pull out of its existing partnerships with Synopsys and/or refuse to participate in future partnerships. This would (i) confer significant competitive advantage to Cadence and Siemens, which would continue to benefit from their existing partnerships with Arm and (ii) hurt Synopsys' overall EDA and S&A business. Secondly, the Notifying Party submits that Cadence, which is active in both design IP, EDA and S&A tools, could respond to any post-Transaction attempts by Synopsys to use Ansys' S&A tools to foreclose it from design IP markets by degrading the interoperability of the Cadence physical verification & sign-off tools with chips incorporating Synopsys' design IP.[752]

(860) Third, the Notifying Party submits that, for the reasons set out at Section 5.4.9.2. above, it is not able to bundle EDA tools and design IP products.[753]

5.4.10.3. The Commission's assessment

5.4.10.3.1. Ability to foreclose

(861) For the reasons set out below, the Commission has reached the conclusion that the Merged Entity **would likely not have the ability** to engage in a strategy of market-wide foreclosure of competing providers of design IP products by totally restricting or degrading interoperability between Ansys' EDA tools and third-party design IP products in any of the relevant affected interoperability pairings specified in Annex A of the Decision, by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings, or by refusing to license Ansys' EDA tools to third-party design IP licensors.

(862) **First**, for the reasons set out at Sections 5.4.5.3.1.1 and 5.4.6.3.1.1 above, the Commission cannot exclude that Ansys holds a significant degree of market power on the worldwide markets for gate-level power integrity analysis with its tool RedHawk(-SC) and electromagnetic simulation with its tool HFSS. Whilst the

751 Form CO, Appendix 1, Intellectual property business, para. 43.
752 Form CO, Appendix 1, Intellectual property business, para. 43.
753 Form CO, paras. 37-38 and Appendix 1, Intellectual property business, paras. 46-47.

Commission cannot exclude that Ansys holds a significant degree of market power in any of the eight other conglomerate leveraging markets because of the significant market shares (see Section 5.4.7.3.1.1), the Commission considers that the market power of these Ansys tools is likely less than that of Ansys' RedHawk(-SC) or HFSS.

(863) **Second**, for the reasons set out below, the commission considers that the Merged Entity **would likely not have the ability** to totally restrict or degrade interoperability between Ansys' EDA tools and third-party design IP products in any of the relevant affected interoperability pairings specified in Annex A of the Decision.

(864) In the first place, as explained at Section 5.4.3.1.1. above, it is crucial for Ansys' EDA tools to interoperate with other EDA tools as well as with design IP products.

(865) In the second place**,** as a competitor stated, since the majority of Ansys' EDA tools relate to verification, it is unlikely that the Merged Entity could substantially degrade the capabilities post-Transaction when the customer uses a competitors' design IP.[754] One reason for this is that design IP products export to EDA tools but there is no export in the opposite direction.[755]

(866) In the third place, Ansys' EDA tools read data exported from design IP products using industry-standard formats. It is therefore difficult to see how interoperability could be restricted or degraded in such a way that Ansys' EDA tools would read data from Synopsys' design IP products but not from third-party design IP products, although all export data using industry-standard formats.

(867) **Third**, for the same reasons as set out Section 5.4.5.3.1.3 above, the Commission considers that it is unlikely that the Merged Entity would have the ability to engage in (pure and/or mixed) bundling between Ansys' EDA tools and Synopsys' design IP products.

(868) **Fourth**, as set out above at Sections 5.4.5 to 5.4.7, it is unlikely that the Merged Entity would have the ability and/or incentive to leverage Ansys' position in the conglomerate leveraging EDA markets to foreclose the Merged Entity's rivals in EDA markets where Synopsys is active. The Commission has no indication that this would be any different as regards the Merged Entity's ability to leverage Ansys' position in the conglomerate leveraging EDA markets to foreclose third-party design IP licensors.

(869) **Fifth**, design IP providers do not need to purchase EDA tools from all vendors or to enter into agreements with the latter to ensure that their design IP interoperates seamlessly with any EDA vendor's tool, because interoperability is presumed between two tools that support industry-standard file formats. In such cases, interoperability is verified through checks EDA vendors / design IP licensors carry out on their own products to ensure that they fully and accurately implement industry standards.[756] Therefore, the Merged Entity could not foreclose a design IP competitor by refusing to license it an EDA tool.

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754 Market participant's response to the European Commission's RFI 2, paragraph 38.

755 Parties' response to the European Commission's RFI 24, Annex Q 2.1.

756 Notifying Party's response to the European Commission's RFI 25, question 30.

(870) In light of the above, and for the purposes of this Decision, the Commission has reached the conclusion that the Merged Entity **would likely not have the ability** to engage in a strategy of market-wide foreclosure of competing providers in design IP markets by totally restricting or degrading interoperability between Ansys' EDA tools and third-party design IP products in any of the relevant affected interoperability pairings specified in Annex A of the Decision, by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings, or by refusing to license Ansys' EDA tools to third-party design IP licensors.

5.4.10.3.2. Incentive to foreclose

(871) For the reasons set out below, the Commission has reached the conclusion that the Merged Entity **would not have the incentive** to engage in a strategy of market-wide foreclosure of competing providers in design IP markets by totally restricting or degrading interoperability between Ansys' EDA tools and third-party design IP products in any of the relevant affected interoperability pairings specified in Annex A of the Decision, by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings, or by refusing to license Ansys' EDA tools to third-party design IP providers.

(872) When considering whether or not to engage in such practices, the Merged Entity faces a trade-off between Ansys' EDA tools forgone and additional or retained sales of Synopsys' design IP products that could otherwise have gone to competitors.

(873) **First,** as regards degradation of interoperability, the results of the market investigation confirmed that such strategy would not be profitable. This is evidenced by the fact that, to the question how they would react if Post-Transaction the Parties were to degrade the interoperability between one or several Ansys' sign-off tools and competitors' (non-Synopsys) design IP products, four times more customers responded that they would switch to sign-off tools and/or design IP products from other providers than customers indicated that they would purchase design IP products and sign-off tools from the Parties.[757]

(874) **Second**, as regards the Merged Entity's incentive to engage in anticompetitive bundling, the Commission considers that this is unlikely for the reasons set out at Section 5.4.9.3.2 above.

(875) **Third**, as regards the Merged Entity's incentive to refuse to license Ansys' EDA tools to third-party design IP providers, it is hard to see how such approach could be profitable given that, since Ansys' EDA tools do not appear to be indispensable for said providers, a refusal to license said tools would only result in lost sales for the Merged Entity, to the benefit of its EDA competitors.

(876) In light of the above, and for the purposes of this Decision, the Commission has reached the conclusion that the Merged Entity would **not have the incentive** to engage in a strategy of market-wide foreclosure of competing providers in design IP markets by totally restricting or degrading interoperability between Ansys' EDA tools and third-party design IP products in any of the relevant affected interoperability pairings specified in Annex A of the Decision, by means of

757 Replies to Questionnaire to customers of EDA and design IP, question D.B.D.1.

anticompetitive (pure and/or mixed) bundling in any bundle pairings, or by refusing to license Ansys' EDA tools to third-party design IP providers.

5.4.10.3.3. Impact on effective competition

(877) Given that the Commission has reached the conclusion that the Merged Entity **would not have the ability or incentive** to engage in a strategy of market-wide foreclosure of competing providers in design IP markets by totally restricting or degrading interoperability between Ansys' EDA tools and third-party design IP products in any of the relevant affected interoperability pairings specified in Annex A of the Decision, or by means of anticompetitive (pure and/or mixed) bundling in any bundle pairings, or by refusing to license Ansys' EDA tools to third-party design IP providers, the Commission has not assessed whether the impact of such foreclosure strategies would lead to a significant impediment to effective competition.

(878) This approach was also confirmed by the results of the market investigation, with a majority of respondents procuring EDA tools not being concerned that the Transaction may impact them negatively or would decrease the intensity of competition in the design IP markets.[758]

5.4.10.3.4. Conclusion

(879) In view of the above considerations and in light of the results of the market investigation and the evidence and information available to it, the Commission concludes that the Transaction does not raise serious doubts as to its compatibility with the internal market as a result of conglomerate effects, notably by foreclosing competing providers of design IP products through leveraging of its products in any of the conglomerate leveraging EDA markets, considering that the Merged Entity would not have the ability and incentive to engage in such strategy.

6. COMMITMENTS

6.1. Analytical framework

(880) The following principles from the Merger Regulation and the Commission's Notice on Remedies acceptable under Council Regulation (EC) No 139/2004 and under Commission Regulation (EC) No 802/2004 (the "**Remedies Notice**")[759] apply where parties to a concentration offer commitments with a view of rendering a concentration compatible with the internal market.

(881) Where a notified concentration raises serious doubts as to its compatibility with the internal market, the parties to the concentration may undertake to modify the concentration to remove the grounds for the serious doubts identified by the Commission. Pursuant to Article 6(2) of the Merger Regulation, where the Commission finds that, following modification by the undertakings concerned, a notified concentration no longer raises serious doubts, it shall declare the concentration compatible with the internal market pursuant to Article 6(1)(b) of the Merger Regulation in conjunction with Article 6(2) of the Merger Regulation.

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758 Replies to Questionnaire to customers of EDA and design IP, questions D.B.E.1, E.2 and E.5.

759 OJ C 267, 22.10.2008, p.1.

(882) As set out in the Remedies Notice, the commitments proposed by the parties have to eliminate the competition concerns entirely and have to be comprehensive and effective from all points of view.[760] Moreover, commitments in Phase I can only be accepted where the competition problem is readily identifiable and can easily be remedied. The competition problem therefore needs to be so straightforward, and the remedies so clear-cut, that it is not necessary to enter into an in-depth investigation and that the commitments are sufficient to clearly rule out 'serious doubts' within the meaning of Article 6(1)(c) of the Merger Regulation.[761]

(883) In assessing whether the proposed commitments will maintain effective competition, the Commission considers all relevant factors, including the type, scale and scope of the proposed commitments with reference to the structure and the particular characteristics of the market in which the competition concerns arise, including the position of the parties and other participants on the market.[762] In order for the proposed commitments to comply with those principles, they must be capable of being implemented effectively within a short period of time.[763]

(884) Concerning the type of acceptable commitments, the Merger Regulation gives discretion to the Commission as long as the commitments meet the required standards. Structural commitments will meet the conditions set out above only in so far as the Commission is able to conclude with the requisite degree of certainty, at the time of its decision, that it will be possible to implement them and that it will be likely that the new commercial structures resulting from them will be sufficiently workable and lasting to ensure that effective competition will be maintained.[764] Divestiture commitments are normally the best way to eliminate competition concerns resulting from horizontal overlaps.

(885) The divested activities must consist of a viable business that, if operated by a suitable purchaser, can compete effectively with the Merged Entity on a lasting basis and that is divested as a going concern. The divested business must include all the assets which contribute to its current operation, or which are necessary to ensure its viability and competitiveness and all personnel which is currently employed or which is necessary to ensure the business' viability and competitiveness.[765]

(886) The intended effect of the divestiture will only be achieved if and once the divested business is transferred to a suitable purchaser in whose hands it will become an active competitive force in the market. The potential of a business to attract a suitable purchaser is an important element of the Commission's assessment of the appropriateness of the proposed commitments [766] Even though normally the divestiture of an existing viable stand-alone business is required, the Commission, by observing the principle of proportionality, may also advise the parties to consider the divestiture of businesses which have existing strong links or are partially integrated with businesses retained by the parties and therefore need to be 'carved out' in those respects. Conversely, carving-out a business from the scope of

760 Remedies Notice, paras. 9 and 61.
761 Remedies Notice, para. 81.
762 Remedies Notice, para. 12.
763 Remedies Notice, para. 9.
764 Remedies Notice, para. 10.
765 Remedies Notice, paras. 23-25.
766 Remedies Notice, para. 47.

the commitments can only be accepted by the Commission if it can be certain that, at least at the time when the business is transferred to the purchaser, a viable business on a stand-alone basis will be divested and the risks for the viability and competitiveness caused by the carve-out will thereby be reduced to a minimum.[767]

(887) There are cases where only the proposal of an up-front buyer will allow the Commission to conclude with the requisite degree of certainty that the business will be effectively divested to a suitable purchaser. In such case, the parties have to undertake in the commitments that they are not going to complete the notified operation before having entered into a binding agreement with a purchaser for the divested business, approved by the Commission.[768]

6.2. Initial commitments

(888) In order to render the concentration compatible with the internal market, the Parties have modified the notified Transaction by entering into the commitments that the Notifying Party submitted on 9 December 2024 (the "**Initial Commitments**") pursuant to Article 6(2) of the Merger Regulation.

(889) The Initial Commitments consisted in the divestment to a suitable purchaser(s) of:

(a) Synopsys' entire optical and photonics device simulation business, the Optical Solutions Group (the "**OSG Divestment Business**"), which includes the entirety of Synopsys' optics and photonics software, including *Code V*, *LightTools*, *LucidShape*, *RSoft* and the recently announced *ImSym*. The OSG Divestment Business includes all assets and staff that contribute to the current operation or are necessary to ensure the viability and competitiveness of the OSG Divestment Business, in particular:[769]

- All tangible and intangible assets (including four facilities and necessary equipment);
- Intellectual property rights (including [number of patents] patents, brand names, copyrights and trade secrets as well as any other intellectual property exclusively related to the OSG Divestment Business);[770]
- All licences, permits and authorisations issued by any governmental organisation for the benefit of the OSG Divestment Business;
- All contracts, leases, commitments and customer orders of the OSG Divestment Business;

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767 Remedies Notice, paras. 35-36.

768 Remedies Notice, para. 53.

769 Initial Commitments, paras. 5-7.

770 With respect to intellectual property rights, **first,** [scope and duration of transitional arrangements]. **Second,** [transitional arrangement provisions to ensure that customers of the OSG Divestment Business continue to benefit from interoperability with Synopsys' retained tool, without requiring Synopsys to disclose its proprietary source code]. **Finally,** neither Synopsys nor the suitable purchaser will be able to enforce its IP rights against the other in order to prevent the other party from operating the OSG Divestment Business or the Synopsys retained business, as applicable. This arrangement (which is free of charge) will allow the suitable purchaser to research, develop, produce, sell, use, and otherwise commercialise products and services of the OSG Divestment Business (and natural evolutions of such products and services, including new versions thereof, whether or not sold under the same brand) using Synopsys' retained intellectual property. This excludes intellectual property owned by Ansys, unless the suitable purchaser decides to exercise an option to also include Ansys' intellectual property, including Ansys' optics and photonics patents.

– All customer contracts, credit and other records of the OSG Divestment Business;

– Members of staff, including all employees currently working, full time or part time, on optics and photonics device simulation business activities;

– Key Personnel such as [list of personnel names working in the OSG Divestment Business] whose retention ought to be guaranteed and which the Parties will not be able to solicit for a period of […] years after closing of the sale of the OSG Divestment Business.[771] It will also include all sales resources and operations; and

– Several transitional supply arrangements relate to IT, facilities, misdirected cash payments, data migration, facilities and knowledge transfer.

(b) Ansys' RTL power consumption analysis product *PowerArtist* and related assets (the "**PCA Divestment Business**"), including the business activities comprised of researching, developing, distributing, licensing, selling, marketing, commercializing and otherwise making available the *PowerArtist* product.[772] The PCA Divestment Business includes all assets and staff that contribute to the current operation or are necessary to ensure the viability and competitiveness of the PCA Divestment Business, in particular:

– All intangible assets (including patents and intellectual property rights)[773];

– All licences, permits and authorisations issued by any governmental organisation for the benefit of the PCA Divestment Business;

– All contracts, leases, commitments and customer orders of the PCA Divestment Business;

– All customer contracts, credit and other records of the PCA Divestment Business;

– Members of staff, including all personnel required to effectively operate the PCA Divestment Business and including at least 40 personnel across Product Management, R&D, and Application Engineering functions;

– Key Personnel such as [list of personnel names working in the PCA Divestment Business] whose retention ought to be guaranteed and

771 Initial Commitments, para. 14 and Initial Commitments, Schedule I, para. 2.12.

772 The PCA Divestment Business also includes the benefit, for the duration of the transitional periods, of all current arrangements under which Ansys supplies products or services to the PCA Divestment Business. Strict firewall procedures will be adopted to ensure that any competitively sensitive information related to, or arising from such supply arrangements will not be shared with, or passed on to, anyone other than for the purpose of the implementation of the Initial Commitments.

773 The Parties and the suitable purchaser will enter into a customary arrangement whereby neither party (Synopsys and/or Ansys and the suitable purchaser) will be able to enforce its IP rights against the other in order to prevent the other party from operating the PCA Divestment Business or the Parties' retained business. With respect to the suitable purchaser, specifically, this arrangement (which will be free of charge) will allow the suitable purchaser to research, develop, produce, sell, use, and otherwise commercialize products and services of the PCA Divestment Business (and natural evolutions of such products and services, including new versions thereof, whether or not sold under the same brand) using the Parties' retained IP.

which the Parties will not be able to solicit for a period of […] years after closing of the sale of the PCA Divestment Business;[774] and

– At the Purchaser's option, the Notifying Party and/or Ansys commits to include at least [number of sales personnel] sales personnel with experience of *Power Artist*.

(890) The OSG Divestment Business and the PCA Divestment Business together form and are jointly referred to as the **"Divestment Businesses"**.

(891) In addition, Synopsys and Ansys have entered into related commitments, inter alia regarding the separation of the divested businesses from their retained businesses, the preservation of the viability, marketability and competitiveness of the divested businesses, including the appointment of a monitoring trustee and, if necessary, a divestiture trustee.

6.3. Assessment of the Initial Commitments

6.3.1. The Notifying Party's views

(892) The Notifying Party submits that the Commitments of the Divestment Businesses will remove the Parties' overlaps in optics and photonics software as well as in RTL power consumption software in full on a global basis.

(893) In the Notifying Party' view, the Divestment Businesses is an attractive, successful, and profitable business.

(894) In addition, as the OSG Divestment Business effectively operates as a standalone business within Synopsys today, it contains everything that a potential purchaser would need to compete effectively. In the same vein, the PCA Divestment Business will include all necessary assets associated with Ansys' RTL PCA tool, *PowerArtist.* As there are no material links between the PCA Divestment Business and the remaining Ansys businesses, the PCA Divestment Business is easily severable.

6.3.2. The results of the market test

(895) The Commission launched a market test of the Initial Commitments on 10 December 2024.

(896) The results of the market test indicated that overall, the sale of the Divestment Businesses would in principle be sufficient to remove the serious doubts raised by the Transaction in the global market for the supply of optics software,[775] the global market for the supply of photonics software[776] and the global market for the supply of RTL power consumption analysis software.[777]

(897) **First,** with regard to the viability of the OSG Divestment Business, a majority of respondents who expressed a view in the Commission's market test of the Initial Commitments consider that the OSG Divestment Business contains all the

774 Initial Commitments, para. 14 and Initial Commitments, Schedule II, paragraph 2 (b).
775 Replies to Questionnaire on remedies market test, question D.12.
776 Replies to Questionnaire on remedies market test, question D.13.
777 Replies to Questionnaire on remedies market test, question E.9.

necessary elements for a suitable purchaser to effectively compete in the global market for the supply of optics software and the global market for the supply of photonics software.[778] Similarly, a majority of respondents who expressed a view in the Commission's market test of the Initial Commitments consider that the PCA Divestment Business contains all the necessary elements for a suitable purchaser to effectively compete in the global market for the supply of RTL power consumption analysis software.[779]

(898) **Second,** with regard to the suitability of the purchaser for the OSG Divestment Business, a majority of respondents to the Commission's market test of the Initial Commitments consider that Keysight Technologies Inc. ("**Keysight**", United States of America), with whom Synopsys entered into a definitive agreement for the sale of the OSG Divestment Business on 3 September 2024, would be a suitable purchaser for the OSG Divestment Business to effectively compete in the global market for the supply of optics software and the global market for the supply of photonics software.[780] For instance, one market participant explained that: "*from a technical perspective they have expertise in related fields and plenty of resources, and if they acquired everything necessary to run the business, they should be able to effectively compete.*"[781]

(899) With regard to the suitability of the purchaser criteria for the PCA Divestment Business, a majority of respondents to the Commission's market test of the Initial Commitments confirmed that the purchaser criteria set out Section D in the Initial Commitments are sufficient for the Commission to approve a purchaser.[782]

(900) **Third,** a majority of respondents to the Commission's market test consider that the Initial Commitments are sufficiently clear and capable of being implemented.[783]

(901) **Fourth,** however, as regards the PCA Divestment Business, market participants expressed very limited interest in acquiring this business.[784]

(902) **Finally,** respondents to the Commission's market test have identified some aspects that should be added to the Initial Commitments in order to improve the viability and competitiveness of the Divestment Businesses, including:

(a) With regard to the suitability of the purchaser of the PCA Divestment Business, some respondents to the Commission's market test consider, in addition to the purchaser criteria already included in the Initial Commitments, that a suitable purchaser would have to be active in the EDA sector or neighbouring markets and already offer EDA tools.[785]

(b) With regard to intellectual property rights, some respondents to the Commission's market test consider that the scope of certain licence-back agreements between the Divestment Business and the Parties' retained

778 Replies to Questionnaire on remedies market test, question D.3.
779 Replies to Questionnaire on remedies market test, question E.3.
780 Replies to Questionnaire on remedies market test, question D.5.
781 Replies to Questionnaire on remedies market test, question D.6.
782 Replies to Questionnaire on remedies market test, question E.4.
783 Replies to Questionnaire on remedies market test, questions D.10 and E.8.
784 Replies to Questionnaire on remedies market test, question E.6.
785 Replies to Questionnaire on remedies market test, question E.4.1.

businesses are too far-reaching and may hamper the ability of the Divestment Business to operate independently from the Parties' retained businesses.[786]

(c) With regard to shared customer contracts, i.e., those customer contracts which relate partly to the OSG Divestment Business or the PCA Divestment Business and partly to the retained Synopsys' or Ansys' businesses, some respondents to the Commission's market test suggested to include *best effort* obligations in splitting existing agreements as well as assurances that intellectual property rights would remain protected, in line with pre-existing agreements.[787]

6.3.3. The Commission's assessment of the Initial Commitments

(903) The Commission considers that the Initial Commitments are sufficient in scope to entirely remove the serious doubts raised by the Transaction in the global market for the supply of optics software, the global market for the supply of photonics software and the global market for the supply of RTL power consumption analysis software as the divestment of the OSG Divestment Business and the PCA Divestment Business completely removes the overlap between the Parties' activities in these markets.

(904) The Commission considers that, based on the evidence on file, and the results of the market test, the Initial Commitments are in general suitable to lead to the divestment of a viable and competitive business, which can compete effectively with the Merged Entity on a lasting basis.

(905) Nevertheless, in order to meet the criteria for an acceptable remedy in Phase I, the Divestment Business needs to be sufficiently standalone and the remedy clear-cut. Therefore, the Commission considers certain amendments to the Initial Commitments to be necessary to ensure that the Divestment Businesses can be operated independently of the Parties as a viable, standalone business by a purchaser(s) and that implementation risks are minimised. In particular:

(a) A clear identification and separation of assets, including with respect to personnel, Key Personnel, shared customer and vendor contracts, IP rights and interoperability agreements needs to be ensured; and

(b) The viability of the Divestment Business needs to be supported by appropriate transitional supply agreements.

(906) Moreover, in view of the feedback from the market test, the Commission considers that the purchaser criteria should reflect the expertise that a suitable purchaser would need to have to effectively operate the PCA Divestment Business, namely by being already active in the EDA sector.

(907) Furthermore, due to the limited interest expressed by market participants in the PCA Divestment Business through the market test, and the expertise necessary for the operation of the PCA Divestment Business, the Commission considers that the Initial Commitments raise implementation risks as to the likelihood that the PCA Divestment Business could be timely divested to a suitable buyer. Implementation safeguards, and particularly an upfront buyer clause, may reduce the risk of delayed implementation of the commitments and provide the requisite degree of

786 Replies to Questionnaire on remedies market test, question C.4.1.

787 Replies to Questionnaire on remedies market test, questions D.1 and E.1.

certainty that the PCA Divestment Business will be effectively and timely divested to a suitable purchaser.

(908) On 19 December 2024, the Commission provided feedback to the Parties on the results of the market test and the Commission's own assessment of the Initial Commitments.

6.4. Assessment of the Final Commitments

(909) On 9 January 2025, the Parties amended the Initial Commitments to take into account the comments received from the Commission based on the feedback from the market test and the Commission's own assessment of the Initial Commitments (the "Final Commitments"). The Final Commitments are annexes to this decision and form an integral part thereof.

(910) The Commission notes that Ansys entered into a definitive agreement for the sale of the PCA Divestment Business to Keysight on 21 December 2024.

(911) The Final Commitments do not contain any substantial changes to the Initial Commitments that would require launching a market test. The Final Commitments contain the following improvements to the Initial Commitments:

(a) An upfront buyer clause is included for each of the OSG Divestment Business and the PCA Divestment Business. Therefore, the Transaction will only be implemented once the Parties have entered into final binding sale and purchase agreements for the sale of the Divestment Businesses and the Commission has approved the suitable purchaser(s) and the terms of sale.

(b) The purchaser criteria specify that the purchaser of the PCA Divestment Business shall be active in the EDA sector.

(c) A more precise and comprehensive list of key personnel and other personnel has been included for both OSG Divestment Business and PCA Divestment Business.

(d) The following clarifications regarding the transfer of customer contracts: first, all customer contracts will be transferred in their entirety to the purchaser(s) of the Divestment Businesses and, second, shared customer contracts will be split in a manner that covers any intellectual property protection rights and pricing terms of the customers concerned.

(e) All interoperability agreements that apply to the software of the Divestment Businesses will be transferred to the purchaser(s) of the Divestment Businesses.

(f) All patents and intellectual property rights exclusively or predominantly used by the Divestment Businesses will be transferred to the purchaser(s) of the Divestment Businesses. While the Final Commitments include a provision that Synopsys and/or Ansys and the purchaser(s) will enter into an arrangement with respect to non-enforcement of certain IP rights, any such arrangement will be limited in scope, set out in the final binding sale and purchase agreement and be subject to the Monitoring Trustee's assessment and the Commission's prior approval.

(g) All agreements to facilitate the migration and operation of the Divestment Businesses by the purchaser(s) will be entered into for a transitional period, and the exact scope and terms will be set out in a transitional services

agreement which will carefully be reviewed by the Commission with the help of the Monitoring Trustee upon the purchaser approval.

(h) The Monitoring Trustee to be appointed shall have relevant experience in the transfer of intellectual property rights.

6.4.1. Suitability of the Final Commitments to remove serious doubts

(912) In light of the results of the market test of the Initial Commitments, the Commission concludes that the Final Commitments are sufficiently clear and suitable to remove the grounds for serious doubts as to the compatibility of the Transaction with the internal market in the global market for the supply of optics software, the global market for the supply of photonics software and the global market for the supply RTL power consumption analysis software, for the following reasons.

(913) **First,** the Commission finds that the submitted remedies are structural in nature and will allow the purchaser(s) to operate in all markets where the Commission raised serious doubts.

(914) **Second,** through the divestment of the OSG Divestment Business, the Final Commitments remove the entire overlap resulting from the Transaction in relation to the global market for the supply of optics software and the global market for the supply of photonics software.[788] Similarly, through the divestment of the PCA Divestment Business, the Final Commitments remove the entire overlap resulting from the Transaction in relation to the global market for the supply RTL power consumption analysis software. On this basis, the Final Commitments remove the entire overlaps in all markets in which the Commission has found that the Transaction may give rise to serious doubts as to its compatibility with the internal market.[789]

(915) **Third,** based on the evidence on file and the results of the market test of the Initial Commitments, the Commission considers that both the OSG Divestment Business and the PCA Divestment Business are standalone businesses, which can compete effectively with the merged entity in the global market for the supply of optics software, the global market for the supply of photonics software and the global

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788 The Commission notes that one respondent to the Commission's market test of the Initial Commitments considers that the OSG Divestment Business should also include tools used in the global market for the supply of photonic chip design software and the global market for the supply of photonic chip simulation software to cover the entire overlap arising from the Transaction in the global market for the supply of photonics software. However, as explained in Section 4.2 above, software in the global market for the supply of photonic chip design software and the global market for the supply of photonic chip simulation software are not part of the global market for the supply of photonics software. As such, the Commission considers that the OSG Divestment Business removes the entire overlap arising from the Transaction in the global market for the supply of photonics software, irrespective of whether software in the global market for the supply of photonic chip design software and the global market for the supply of photonic chip simulation software are included within the scope of the OSG Divestment Business.

789 The Commission notes that, contrary to claims made by a minority of respondents to the Commission's market test of the Initial Commitments, the mere fact that certain products included in the Divestment Businesses may have lost traction over the past years and/or constitute legacy products is without bearing on the fact that the Final Commitments remove the entire overlap arising from the Transaction in the global market for the supply of optics software, the global market for the supply of photonics software and the global market for the supply of RTL power consumption analysis software.

market for the supply RTL power consumption analysis software respectively. Indeed, (i) the majority of respondents to the Commission's market test of the Initial Commitments consider that the OSG Divestment Business contains all the necessary elements to enable a suitable purchaser to effectively compete in the global market for the supply of optics software;[790] (ii) the majority of the respondents to the Commission's market test of the Initial Commitments consider that the OSG Divestment Business contains all the necessary elements to enable a suitable purchaser to effectively compete in the global market for the supply of photonics software;[791] and, (iii) the majority of the respondents to the Commission's market test of the Initial Commitments consider that the PCA Divestment Business contains all the necessary elements to enable a suitable purchaser to effectively compete in the global market for the supply of RTL power consumption analysis software.[792]

(916) **Fourth,** in order to meet the criteria for an acceptable remedy in Phase I, the divestment business needs to be sufficiently standalone, and the remedy clear-cut. Moreover, the divestment business must be capable of being implemented effectively within a short period of time and thus any implementation risks identified by the Commission or raised by the market participants in the market test should be minimised. In this case, the Divestment Businesses is composed of assets that are carved out of (i) the wider Synopsys organisation in relation to the OSG Divestment Business; and, (ii) the wider Ansys organisation in relation to the PCA Divestment Business, and the transfer of some assets requires the consent of third parties, including customers.[793] Based on the results of the market test[794] and given the improvements made in the Final Commitments, the implementation of the Final Commitments would not raise additional risks.

(917) For the reasons outlined above, the Final Commitments entered into by Synopsys and Ansys are therefore sufficient to clearly rule out serious doubts as to the compatibility of the Transaction with the internal market.

6.4.2. Viability and competitiveness of the Divestment Businesses

6.4.2.1. Viability and competitiveness of the OSG Divestment Business

(918) The Commission considers that the OSG Divestment Business is a viable and competitive business for the following reasons.

(919) **First,** the OSG Divestment Business is growing and profitable, with a turnover of USD [70-90 million] in 2023, which are expected to grow to USD [110-130] in 2028. Furthermore, the operating margin of the OSG Divestment Business is of approximately […]%.[795]

(920) **Second,** the OSG Divestment Business has attracted a significant interest from a number of potential purchasers, including industrial and financial purchasers.[796]

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790 Replies to Questionnaire on remedies market test, question D.3.
791 Replies to Questionnaire on remedies market test, question D.3.
792 Replies to Questionnaire on remedies market test, question E.3.
793 [Synopsys rationale for offering to divest Ansys' RTL power consumption software].
794 Replies to Questionnaire on remedies market test, questions D.2 and E.2.
795 Form RM, paras. 2.3 and 4.17-4.19.
796 Form RM, para. 2.3.

(921) **Third,** the market test confirmed the viability and the competitiveness of the OSG Divestment Business. The majority of respondents to the market test of the Initial Commitments confirmed that the OSG Divestment Business would be viable and would allow a suitable purchaser to compete effectively and on a lasting basis in the global market for the supply of optics software and in the global market for the supply of photonics software.[797]

(922) **Fourth,** while some market participants have expressed concerns about customer or vendor contracts,[798] the Commission notes that (i) for customers of the OSG Divestment Business only, the agreements will be entirely assigned and, consequently, transferred to a suitable purchaser with all the conditions and obligations contained therein; and, (ii) the Final Commitments contain express provisions for the Notifying Party to split any shared customer contract in such a way that covers any intellectual property protection rights and pricing terms of the customers concerned and after the OSG Divestment Business is divested to a suitable purchaser, the optics and photonics software will be provided by the suitable purchaser, whereas other services will continue to be provided by Synopsys.[799]

(923) Furthermore, as regards shared vendor agreements, the Notifying Party submits that [30-40]% of vendor agreements are shared. While none of these shared vendor agreements will be transferred to the OSG Divestment Business, the Notifying Party submits that those services will be offered to the OSG Divestment Business by relying on existing vendor agreements of the suitable purchaser of the OSG Divestment Business.[800]

(924) **Fifth,** while some market participants consider that interoperability agreements between software of the purchaser and the vendors or the purchaser and other suppliers in the global markets for the supply of optics and photonics software will need to be continued after the divestment, the Commission notes that the Final Commitments include a clause ensuring that all interoperability agreements that apply to the software of the OSG Divestment Business will be transferred to the purchaser of the OSG Divestment Business.[801]

(925) **Sixth,** while some market participants have expressed concerns with regard to the material intellectual property right links that will remain between the OSG Divestment Business and Synopsys' retained businesses, the Commission notes that such clauses have been amended in the Final Commitments and solve the risks highlighted during the market test of the Initial Commitments.

(926) First, all patents and intellectual property rights exclusively or predominantly used by the OSG Divestment Business will be transferred to the purchaser of the OSG Divestment Business.[802] In addition, the Parties and the purchaser will also enter into a customary arrangement whereby the Parties and the purchaser will agree not to enforce intellectual property rights. In that respect, Synopsys will agree not to enforce its retained IP rights against the purchaser in order to prevent it from

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797 Replies to Questionnaire on remedies market test, question D.3.

798 Including, where relevant, in relation to existing intellectual property rights and non-disclosure agreements where applicable.

799 Final Commitments, Schedule I, para. 3.1.

800 Final Commitments, Schedule I, para. 3.1.

801 Final Commitments, Schedule I, para. 2.10.

802 Final Commitments, Schedule I, paras. 2.3 and 2.5.

operating the OSG Divestment Business, and the purchaser will agree not to enforce IP rights transferred with the OSG Divestment Business to the extent any such rights are used in or necessary for the operation of the retained business' activities that are unrelated to the activities of the OSG Divestment Business. Such customary arrangement will be set out in the sale and purchase agreement, which will be carefully reviewed by the Commission with the help of the Monitoring Trustee during the purchaser approval process.[803]

(927) Second, the agreements to facilitate the migration and operation by the purchaser of the OSG Divestment Business will be entered into for a transitional period. The exact scope and terms of transitional agreements will be set out in a transitional services agreement which will be carefully reviewed by the Commission with the help of the Monitoring Trustee upon the purchaser's approval.

(928) On the basis of the above, the Commission concludes that the OSG Divestment Business is a viable and competitive business.

6.4.2.2. Viability and competitiveness of the PCA Divestment Business

(929) The Commission considers that the PCA Divestment Business is a viable and competitive business for the following reasons.

(930) **First,** the PCA Divestment Business is profitable, with a turnover of USD [15-20 million] in 2023,[804] which is expected to grow to USD [25-30] by 2027. Furthermore, the direct contribution margin was of approximately […]% in the last three years.[805]

(931) **Second,** the market test confirmed the viability and the competitiveness of the PCA Divestment Business. The majority of respondents to the market test of the Initial Commitments confirmed that the PCA Divestment Business would be viable and would allow a suitable purchaser to compete effectively and on a lasting basis in the global market for the supply of RTL power consumption analysis software.[806]

(932) **Third**, some respondents to the Commission' market test of the Initial Commitments consider that a suitable purchaser of the PCA Divestment Business would have to be active in neighbouring markets and already offers EDA tools. The Commission notes that the Final Commitments specify in the purchaser criteria that the suitable purchaser will be already active in the EDA sector, which will allow it to better compete as it already offers a suite of EDA tools.[807]

(933) **Fourth**, while some market participants have expressed concerns about customer and vendor contracts,[808] the Commission notes that (i) for customers of the PCA Divestment Business only, the agreements will be entirely assigned and, consequently, transferred to a suitable purchaser with all the conditions and obligations contained therein; and, (ii) the Final Commitments contain express provisions for the Notifying Party and Ansys to split any shared customer contract

803 Final Commitments, Schedule I, para. 2.6.
804 Form RM, para. 4.24.
805 Form RM, footnote 32.
806 Replies to Questionnaire on remedies market test, question E.3.
807 Final Commitments, para. 18.
808 Including, where relevant, in relation to existing intellectual property rights and non-disclosure agreements where applicable.

in such a way that covers any intellectual property protection rights and pricing terms of the customers concerned and after the PCA Divestment Business is divested to a suitable purchaser, the RTL power consumption software will be provided by the suitable purchaser, whereas other services will continue to be provided by Ansys.[809]

(934) Furthermore, for shared vendor agreements, the Notifying Party and Ansys will use best efforts and cooperate in good faith with the purchaser to facilitate the execution of a new contract between the purchaser and the applicable vendor, or Ansys will transfer its rights in such vendor contract to the extent related to the PCA Divestment Business to the purchaser.[810]

(935) **Fifth**, while some market participants consider that interoperability agreements between software of the purchaser and the vendors or the purchaser and other suppliers in the global market for the supply of RTL power consumption analysis software will need to be continued after the divestment, the Commission notes that the Final Commitments include a clause ensuring that all interoperability agreements that apply to the software of the PCA Divestment Business will be transferred to the purchaser of the PCA Divestment Business.[811]

(936) **Sixth,** while some market participants have expressed concerns with regard to the material intellectual property right links that will remain between the PCA Divestment Business and Synopsys' retained business, the Commission notes that such clauses have been amended in the Final Commitments and solve the risks outlined by the market test. First, all patents and intellectual property rights exclusively or predominantly used by the PCA Divestment Business will be transferred to the purchaser of the PCA Divestment Business.[812]

(937) In addition, the Parties and the purchaser will also enter into a customary arrangement whereby the Parties and the purchaser will agree not to enforce intellectual property rights. In that respect, Ansys will agree not to enforce its retained IP rights against the purchaser in order to prevent it from operating the PCA Divestment Business, and the purchaser will agree not to enforce IP rights transferred with the PCA Divestment Business to the extent any such rights are used in and necessary for the operation of the retained business' activities unrelated to the activities of the PCA Divestment Business. Such customary arrangement will be set out in the sale and purchase agreement, which will be carefully reviewed by the Commission with the help of the Monitoring Trustee during the purchaser approval process.[813]

(938) Second, the agreements to facilitate the migration and operation by the purchaser of the PCA Divestment Business will be entered into for a transitional period. The exact scope and terms of transitional agreements will be set out in a transitional services agreement which will be carefully reviewed by the Commission with the help of the Monitoring Trustee upon the purchaser's approval.

809 Final Commitments, Schedule II, para. 2(d).
810 Final Commitments, Schedule II, para. 2(d).
811 Final Commitments, Schedule II, para. 2(d).
812 Final Commitments, Schedule II, para. 2(b).
813 Final Commitments, Schedule II, para. 2(h).

(939) On the basis of the above, the Commission concludes that the PCA Divestment Business is a viable and competitive business.

6.4.3. Conclusion on the Final Commitments

(940) The Commission considers that the improvements made in the Final Commitments adequately address the shortcomings identified with respect to the Initial Commitments.

(941) Based on the results of the market test and the Commission's assessment of the Initial Commitments and the Final Commitments, the Commission considers that the Final Commitments entirely remove the Commission's serious doubts as to the compatibility of the Transaction with the internal market.

7. CONDITIONS AND OBLIGATIONS

(942) Pursuant to the second subparagraph of Article 6(2) of the Merger Regulation, the Commission may attach to its decision conditions and obligations intended to ensure that the undertakings concerned comply with the commitments they have entered into vis-à-vis the Commission with a view to rendering the concentration compatible with the internal market.

(943) The fulfilment of the measure that gives rise to the structural change of the market is a condition, whereas the implementing steps which are necessary to achieve this result are generally obligations on the Parties. Where a condition is not fulfilled, the Commission's decision declaring the concentration compatible with the internal market is no longer applicable. Where the undertakings concerned commits a breach of an obligation, the Commission may revoke the clearance decision in accordance with Article 6(3)(b) of the Merger Regulation. The undertakings concerned may also be subject to fines and periodic penalty payments under Articles 14(2) and 15(1) of the Merger Regulation.

(944) In accordance with the basic distinction described in the previous paragraph as regards conditions and obligations, this decision should be made conditional, on the one hand, on the full compliance by the Parties with Section B (including Schedules 1 and 2) of the Final Commitments submitted by the Parties on 9 January 2025. All other Sections of the Final Commitments should be obligations within the meaning of Article 6(2) of the Merger Regulation. The full text of the Final Commitments is attached as Annex B to this decision and forms an integral part thereof.

8. CONCLUSION

(945) For the above reasons, the Commission has decided not to oppose to the notified operation as modified by the commitments and to declare it compatible with the internal market and with the functioning of the EEA Agreement, subject to full compliance with the conditions in sections Section B (including Schedules 1 and 2) of the commitments annexed to the present decision and with the obligations contained in the other sections of the said commitments. This decision is adopted in application of Article 6(1)(b) in conjunction with Article 6(2) of the Merger Regulation and Article 57 of the EEA Agreement.

For the Commission

(Signed)
Teresa RIBERA
Executive Vice-President

M.11481 – SYNOPSYS / ANSYS

Commission decision pursuant to Article 6(1)(b) in conjunction with Article 6(2) of Council Regulation No 139/2004 and Article 57 of the Agreement on the European Economic Area

Annex A – Product mapping and Interoperability

Contents

1 INTRODUCTION 2

2 NO ADEQUATE EXTERNAL SOURCES FOR THE COMPUTATION OF EDA MARKET SHARES 2

3 PRODUCT MAPPING AND EDA MARKET SHARES 4

3.1 Product mapping – design-flow combination level (Segment ID level) 4

3.2 Product mapping – functional level (Functional ID level) 15

3.3 Revenue and market size data 17

3.3.1 The Parties' revenues for their own products 17

3.3.2 The Parties' best estimates of segment sizes 18

3.3.3 The Parties' best estimates of rivals' revenues 18

3.4 Market shares at the functional level (Functional ID level) 19

4 INTEROPERABILITY MATRIX (EDA AND DESIGN IP) 21

4.1 Interoperability relationships between EDA and Design IP 21

4.2 EDA functions without interoperability relationships 29

1 INTRODUCTION

(1) This Annex describes third-party sources for Electronic Design Automation (EDA) revenues (Section 2) and Synopsys' and Ansys' (together the Parties') Product Mapping exercise that mapped EDA tools and revenues to different EDA segments (Section 3). In addition, this Annex describes the interoperability matrix developed to assess the interoperability relationships between EDA tools (Section 4).

(2) **Product mapping exercise**. During the Commission's investigation, the Notifying Party submitted that the EDA market should be segmented according to EDA functions.[1] Market participants highlighted that different types of chips, notably digital and analog chips, require specialised EDA design tools. In addition, chip design flows have different design stages, like design, verification and sign-off, that require specialised tools.

(3) Calculating market shares for EDA segments is not straightforward, because third-party sources do not segment the EDA market with regard to EDA functions, the design flows for different types of chips (digital, analog, mixed-signal, multi-die and photonic chips) and design stages. In addition, the data gathered from EDA vendors is incomplete and often extrapolated.[2]

(4) To address these limitations of external sources, the Commission engaged the Parties in a substantive effort to map EDA tools to different market segments. This was complemented by a market reconstruction exercise to gather views on market segmentation and revenue data by the Parties' main competitors in EDA.[3]

(5) **Interoperability matrix.** The design of semiconductor chips requires the use of many different EDA tools with complementary functions. However, there are no external data sources mapping the interoperability relationships (i.e. the transmission of data) between these EDA functions.

(6) As basis for the assessment of interoperability, the Commission requested the Parties to map the data exchange between EDA functions in different chip design flows and to explain whether this data exchange is based on proprietary data formats or industry standards (possibly supported by interoperability agreements).

2 NO ADEQUATE EXTERNAL SOURCES FOR THE COMPUTATION OF EDA MARKET SHARES

(7) The Commission considers that there are no adequate external data sources for the computation of market shares in the EDA market, for the reasons set out below.

(8) **First**, the Notifying Party submits that quarterly reports prepared by the **Electronic System Design Alliance (ESDA)**, the EDA industry association are the best available external source of EDA revenues. However, this data is not adequate to estimate market shares.

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1 See, Decision, Section, 4.2.1.2; Form CO, paras. 301-303.

2 To the contrary, external market share sources were available for Design IP (IPNest, cf Form CO, Section 1-5 Appendix 1, Table 3, FN 1629) and the optics and photonics markets (LP Information, cf Form CO, para 947).

3 Market participants' response to the European Commission's RFI 1 and 3.

(9) In the first place, Synopsys relies on ESDA in the ordinary course of business to inform its quarterly business reviews and strategic planning.[4] Synopsys estimates segment sizes and shares across different EDA segments in an internal database [information on Synopsys' market intelligence].[5]

(10) In the second place, Ansys also relies on quarterly ESDA reports, the S&A Market Analysis Report Series by CIMdata, quarterly updates from ESDA in the ordinary course of business. In addition, Ansys uses [information on Synopsys' market intelligence].[6]

(11) In the third place, the Notifying Party submits that ESDA extrapolates missing data based on outdated information.[7]

(12) Firstly, Synopsys provides [description of Synopsys practice in providing data to ESDA and market intelligence on ESDA methodology in estimating Synopsys revenues].[8]

(13) Secondly, Ansys [description of Ansys practice in providing data to ESDA]. Ansys is […] not included in the majority of ESDA market size estimates. According to Ansys, [Ansys market intelligence regarding ESDA methodology in estimating Ansys revenues].[9]

(14) In the fourth place, the Notifying Party submits that "[Synopsys' market intelligence]. *This is because ESDA categories (which were historically defined by ESDA) do not reflect how competition occurs in the market and group revenues from tools that do not compete in practice.*"[10]

(15) **Second,** some market participants pointed to market share data provided by **Pedestal Research**.[11] However, this data appears inferior to ESDA data and not adequate to estimate market shares.

(16) In the first place, the Notifying Party submits that Pedestal data is outdated and does not reflect current market structure. Pedestal Research's latest publicly available EDA market report would have been published in 2018 and the firm would not appear to be currently active. In that regard, the Commission notes that the latest report announced on the Pedestal Research website indeed seems to be from 2018.[12] Other market participants referenced a Pedestal report from 2023 based on 2021 data and updated EDA shares from March 2024, based on 2022 data[13] While these reports indicate that Pedestal Research may still be active, they also suggest that Pedestal reports are not based on current data.

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4 Form CO, para 170.
5 Form CO, para 349.
6 Form CO, para 171.
7 Form CO, para 350, Reply to RFI 7, paras 1.1-1.2.
8 Reply to RFI 7, para 1.1.
9 Reply to RFI 7, para 1.2.
10 Reply to RFI 7, para 351.
11 Siemens' submission of 14 June 2024, "*Acquisition Of Ansys By Synopsys – European Commission Voluntary Submission - Siemens*", Cadence's Reply to RFI 3 of 27 November 2024 also makes reference to Pedestal.
12 http://pedestalresearch.com/research/, accessed 5 November 2024.
13 Market participants' submissions and response to the European Commission's RFI 3.

(17) In the second place, the Notifying Party submits that [Parties' market intelligence practice].[14] In that regard, the Commission notes that the Pedestal reports and tables referenced by other market participants do not state data sources.[15]

(18) **Third**, there are no other external sources that could be used for the computation of EDA market shares.

(19) In the first place, the Notifying Party submits that **International Business Strategies, Inc (IBS)**, publishes monthly reports and industry outlook reports on the semiconductor industry. [Parties' market intelligence practice]. The July 2024 report submitted by the Parties would contain a "*high level overview of the EDA segment based on publicly available information as well as Dr. Handel H. Jones' general market expertise*".[16] The Commission notes that this report contains revenue estimates for "CAE", "IC physical design" and "PCB/MCM" (Printed circuit board/multi-chip module") and several Design IP market segments. In addition, the report contains company level revenue estimates for Synopsys, Cadence, Siemens , Ansys and Keysight. However, their revenues were not further broken down across EDA segments.

(a) In the second place, the Notifying Party submits that **Cambashi** is a global market research, industry analysis, consulting and training firm, focused on engineering and industrial software. To the best of Synopsys' understanding, Cambashi provides share, size, and forecast data for "*Computer Aided Engineering*" which would not cover EDA. The Notifying Party understands that Cambashi's definition of "*Computer Aided Engineering*" may apply to physics simulation software, such as fluid dynamics, multi-physics, thermal, acoustic, and other types of simulation. [Parties' market intelligence practice].

(20) In the third place, the Notifying Party submits that **CIMdata**, a market intelligence source company dated 1983, also reports information on PLM. [Parties' market intelligence practice]. To the best of the Parties' knowledge, CIMdata largely relies on self-reporting and public information. In that regard, the Commission notes that the CIMData Report of July 2022 submitted by the Notifying Party does not contain a breakdown of EDA revenues[17] and seems to overstate total EDA revenues.[18]

3 PRODUCT MAPPING AND EDA MARKET SHARES

3.1 Product mapping – design-flow combination level (Segment ID level)

(21) In order to compute EDA market shares, the Commission requested the Parties to complete a template mapping their and their competitors' products to each '*design flow*

14 Reply to RFI 7, para 1.3.
15 Market participants' submissions and response to the European Commission's RFI 3.
16 Reply to RFI 7, Annex Q 1.34.
17 Reply to RFI 1, Annex RFI Q-36-001.
18 For example, the total EDA revenue in 2021 is estimated at USD 11.4bn, while the Notifying Party submits a total revenue of USD 8.7bn in 2021, Form CO, Table 16.

combination'[19] within the EDA sector (including photonic chips) as well as mapping EDA-related categories falling outside the design flow and Design IP.[20]

(22) Design flow combinations are unique combinations of the following four types of categories: design flow, presentation, design stage, and function.

(a) **Design flow (Level 0 – L0):** Reflects the type of IC and semiconductor device for the design of which a product is used: (i) Digital Design Flow, (ii) Analog Design Flow, (iii) Mixed-signal Design Flow, (iv) Photonic Design Flow, (v) Multi-die chip Design Flow, (vi) PCB Design Flow, (vii) Packaging Design Flow.

(b) **Presentation (Level 1 – L1):** This category includes the "front-end" and "back-end" of the design flow.[21] However, these terms are not used by all market participants. In addition, as design stages (introduced in lit c below) do not overlap across presentation, this category is not strictly needed for the segmentation of the EDA market and for defining a unique design flow combination.

(c) **Design stage (Level 2 – L2):** This sub-category includes the different stages of the design flow. Earlier stages generally concern the design of a chip, while later stages concern the verification. For illustration, the Digital Design Flow (Annex A, Table 2) front-end includes the stages "*Architectural Design*", i.e. a high level logical design of the chip, "*Logic/Circuit Design*", a more detailed logical design of the chip and "*Functional Verification*", that ensures that the logical design is correct. The back-end includes the stages "*Physical Design*", i.e. the translation of the logical design into the physical design of a silicon die and "*Physical Verification & Sign-off*" that ensures the physical design works as intended.

(d) **Function (Level 3 – L3):** This category includes the specific functions of EDA tools within each design stage. For example, functions in the "*Physical Verification & Sign-off*" stage of the Digital Design Flow include "*Gate-level Power Integrity Analysis*". This is considered the **level 3 (L3)** of the design flow.

(23) The Parties identified the **functionalities** of their products and allocated them to design flow combinations within the EDA design flow following an approach reflecting demand-side substitutability considerations. While most functionalities appear only in one design flow, a number of functionalities appears in multiple design flows and stages. For example, "*Circuit Simulation*" appears in the Analog Design Flow, Pre-Layout Simulation and Post-Layout Simulation, and in the Multi-die Chip Design Flow, Pre-Layout Simulation and Post-Layout Simulation.

(24) In addition to functions (and products) falling within the design flows, the Parties also identified EDA and EDA-adjacent categories that fall **outside of the design flow**. These have been assigned the label "*Outside of the design flow*" in each of the flow level 0, flow level 1, flow level 2 fields. Products falling outside of the design flow have been assigned their corresponding CRES labels in the level 3 field.

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19 These are unique combinations of design flow, presentation, design stage, and function.

20 Design IP was included in the product mapping to facilitate the mapping of interoperability links between Design IP and EDA tools in a unified framework. However, Design IP segments and market shares are based on an external data source. See Decision,

21 The front-end concerns the logical design of a chip, while the back-end concerns the translation of this conceptual design into a physical design of the chip on a silicon die.

(25) In addition to EDA segments, the Parties extended this exercise to Design IP. These haven been assigned the label "**Design IP**" in level 0-2. Contrary to EDA, Design IP segments (level 3) and revenues are based on external data.[22]

(26) The product mapping exercise identified **88 design flow combinations** in EDA, uniquely identified by a design flow (L0), design stage (L2) and EDA function (L3) and indexed by a unique numerical identifier, the **Segment ID.**[23] Including Design IP segments, there is a total of **97 design flow combinations**.

(27) The structure of the EDA Product Mapping (L0-L2) submitted by the Parties is displayed in **Table 1**. **Tables 2-7** map EDA tools and Design IP to different design flow combinations:

a. **Table 2** lists segments and tools in the Digital design flow (Segment IDs 1-31);

b. **Table 3** lists segments and tools in the Analog design flow (Segment IDs 32-51);

c. **Table 4** lists segments and tools in the Mixed-signal design flow (Segment IDs 52-53), Photonic chips design flows (Segment IDs 54-57);

d. **Table 5** lists segments and tools in the Multi-die design flow (Segment IDs 58-77);

e. **Table 6** lists segments and tools in the PCB (Segment IDs 78-79), Packaging (Segment ID 80) & Outside of Design Flows (Segment IDs 81-87);

f. **Table 7** lists Design IP segments (89-97).

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22 To the contrary, external market share sources were available for Design IP (IPNest, cf Form CO, Section 1-5 Appendix 1, Table 3, FN 1629)

23 For example, "*Gate-level Power Integrity Analysis*" is Segment ID 30.

Table 1. EDA Product Mapping (design-flow combinations).

Segment IDs	**Level 0** *Design flow or offering*	**Level 1** *Presentation*	**Level 2** *Design Stage*	**Level 3** *Function/Segment*	**Market size 2023 (USD[…])**
1-4	**Digital Design Flow**	Front-end	Architectural Design	4 functions	[…]
5-11		Front-end	Logic / Circuit Design	7 functions	
12-17		Front-end	Functional Verification	6 functions	
18-20		Back-end	Physical Design	3 functions	
21-31		Back-end	Physical Verification & Sign-off	11 functions	
32	**Analog Design Flow**	Front-end	Schematic Design	1 function	[…]
33-34		Front-end	Pre-Layout Simulation	2 functions	
35-36		Back-end	Layout	2 functions	
37		Back-end	Physical Design	1 function	
38-49		Back-end	Physical Verification & Sign-off	12 functions	
50-51		Back-end	Post-Layout Simulation	2 functions	
52	**Mixed-signal Design Flow**	Front-end	Co-Simulation	1 function	[…]
53		Back-end	Co-Design	1 function	
54-56	**Photonic Design Flow**	Front-end	Schematic Design	3 functions	[…]
57		Back-end	Post-Layout Simulation	1 function	
58	**Multi-die chip Design Flow**	Front-end	Pre-Layout Simulation	1 function	[…]
59-60		Front-end	Architectural Design	2 functions	
61-63		Front-end	Logic / Circuit Design	3 functions	
64-68		Front-end	Functional Verification	5 functions	
69-76		Back-end	Physical Verification & Sign-off	8 functions	
77		Back-end	Post-Layout Simulation	1 function	
78-79	**PCB Design Flow**	Back-end	Verification	2 functions	[…]
80	**Packaging Design Flow**	Back-end	Verification	1 function	[…]
81-87	**Outside of Design Flow**			7 functions	[…]
88	**Revenue from legacy EDA products**			N/A	[…]
89-97	**Design IP**			9 segments	[…]
			Total EDA (USDM, 2023)		[…]
			Total EDA+Design IP (USDM, 2023)		[…]

Source: Reply to RFI 19, Annex Q.3.1, Commission assessment.

Table 2. Segments and tools in the Digital Design Flow.

Level 1	Level 2	Level 3	Segment ID	Market size (USD […])	List of tools
Front-end	Architectural Design	High-Level Synthesis	1	[…]	CADENCE (Stratus), SIEMENS (Catapult)
		RTL Analysis	2	[…]	SYNOPSYS (RTL Architect); CADENCE (RTL Joules Studio); SIEMENS (Unknown)
		RTL Power Consumption Analysis	3	[…]	SYNOPSYS (PrimePower RTL; SpyGlass Power); ANSYS (PowerArtist); CADENCE (Joules RTL; Palladium DPA); SIEMENS (PowerPro; Veloce Power)
		Early Architectural Exploration	4	[…]	SYNOPSYS (Platform Architect); CADENCE (Interconnect Workbench); SIEMENS (Vista Flow); KEYSIGHT (Unknown); MATHWORKS (Unknown); ZUKEN (Unknown)
	Logic / Circuit Design	RTL Synthesis	5	[…]	SYNOPSYS (Design Compiler; Power Compiler); CADENCE (Genus); SIEMENS (Oasys RTL)
		FPGA Synthesis	6	[…]	SYNOPSYS (Synplify); SIEMENS (Precision); ALTERA (Quartus); AMD (Vivado)
		Static Verification	7	[…]	SYNOPSYS (VC SpyGlass); CADENCE (JasperLint); SIEMENS (Questa Lint/CDC); REAL INTENT (Ascent AutoFormal; Ascent Lint; Meridian CDC; Meridian RDC)
		Gate-level Power Consumption Analysis	8	[…]	SYNOPSYS (PrimePower); CADENCE (Joules)
		Timing Constraints	9	[…]	SYNOPSYS (SpyGlass Constraints; Timing Constraints Manager); CADENCE (Conformal Litmus); AUSDIA (TimeVision Platform); EXCELLION (ConCert; ConMan; ConStruct; ConTree)
		Silicon Lifecycle Management IP	10	[…]	SYNOPSYS (Synopsys SLM CDM IP; Synopsys SLM HSAT IP; Synopsys SLM PMM IP; Synopsys SLM PVT IP; Synopsys SLM XLBIST IP); SIEMENS (Tessent Embedded Analytics); PROTEANTECS (Agents)
		Design-for-Test / Test IP	11	[…]	SYNOPSYS (DFT Compiler; Synopsys SLM SHS IP; Synopsys SLM SMS IP; TestMAX Access; TestMAX Advisor; TestMAX DFT; TestMAX LBIST Add-on; TestMAX Manager; TestMAX SMS); CADENCE (Modus); SIEMENS (Tessent); SYNTEST (DFT-PRO; TurboBIST; TurboSCAN)
	Functional Verification	Simulation Verification	12	[…]	SYNOPSYS (VCS; VIP; VSO.ai; Z01X); CADENCE (VIP; Xcelium); SIEMENS (Questa; VIP); CAST (Unknown)
		Debug Verification	13	[…]	SYNOPSYS (Euclide; VC Execution Manager; Verdi); CADENCE (Verisium (aka Indago)); SIEMENS (Questa Visualizer)
		Formal Verification	14	[…]	SYNOPSYS (VC Formal); CADENCE (JasperGold); SIEMENS (Questa Formal & OneSpin); VENNSA (Unknown)
		Static Verification	15	[…]	SYNOPSYS (VC SpyGlass); CADENCE (JasperLint); SIEMENS (Questa Lint/CDC); REAL INTENT (Ascent AutoFormal; Ascent Lint; Meridian CDC; Meridian RDC)
		Emulation-Based Power Analysis	16	[…]	SYNOPSYS (ZeBu Empower); CADENCE (Palladium DPA)
		Hardware-Assisted Verification	17	[…]	SYNOPSYS (HAPS; Threadmill; ZeBu); CADENCE (Palladium/Protium); SIEMENS (Veloce CS)

Level 1	Level 2	Level 3	Segment ID	Market size (USD […])	List of tools
Back-end	Physical Design	Place & Route	18	[…]	SYNOPSYS (DSO; Fusion Compiler; IC Compiler; IC Compiler II; RedHawk Analysis Fusion); CADENCE (Innovus); SIEMENS (Aprisa); EMPYREAN (Unknown)
		Timing Constraints	19	[…]	SYNOPSYS (Timing Constraints Manager); CADENCE (Conformal Litmus); AUSDIA (TimeVision Platform); EXCELLION (ConCert; ConMan; ConStruct; ConTree)
		Equivalence Checking	20	[…]	SYNOPSYS (Formality); CADENCE (Conformal); SIEMENS (OneSpin)
	Physical Verification & Sign-off	Physical Verification	21	[…]	SYNOPSYS (IC Validator); CADENCE (Pegasus); SIEMENS (Calibre); KEYSIGHT (Unknown); EMPYREAN (Argus); SILVACO (Unknown)
		ESD Analysis	22	[…]	SYNOPSYS (ICV PERC; PrimeESD); ANSYS (PathFinder (+SC)); CADENCE (PVS-PERC; Pegasus-PERC; Voltus ESD); SIEMENS (Calibre PERC); KEYSIGHT (Unknown); ANGSTROM DESIGN AUTOMATION (DECIMM); DASSAULT (CST Studio); MAGWEL (ESDi); SILVACO (Unknown)
		Timing Analysis	23	[…]	SYNOPSYS (PrimeTime); CADENCE (Tempus); SIEMENS (Unknown); EMPYREAN (XTime)
		ECO	24	[…]	SYNOPSYS (PrimeClosure; Tweaker); CADENCE (Tempus ECO); SIEMENS (Unknown); EMPYREAN (Xtop)
		Clock Jitter Analysis	25	[…]	ANSYS (ClockFX); CADENCE (Tempus); SIEMENS (Unknown)
		Parasitic Extraction	27	[…]	SYNOPSYS (StarRC); CADENCE (Quantus Extraction); SIEMENS (Calibre xRC); EMPYREAN (Empyrean RCExplorer)
		Design Robustness	29	[…]	SYNOPSYS (PrimeShield); CADENCE (Tempus Design Robustness); SIEMENS (Unknown)
		Gate-level Power Integrity Analysis	30	[…]	ANSYS (RedHawk (+SC)); CADENCE (Voltus); SIEMENS (mPower)
		Gate-level Security Analysis	31	[…]	ANSYS (RedHawk-SC Security)

Source: Reply to RFI 19, Annex Q.3.1.

Table 3. Segments and tools in the Analog Design Flow.

Level 1	Level 2	Level 3	Segment ID	Market size (USD […])	List of tools
Front-end	Pre-Layout Simulation	Schematic Editing	32	[…]	SYNOPSYS (Custom Compiler); CADENCE (Virtuoso Schematic Editor); SIEMENS (Taner); KEYSIGHT (ADS); EMPYREAN (Aether); SIGASI (Unknown); SILVACO (Unknown)
		Circuit Simulation	33	[…]	SYNOPSYS (PrimeSim Continuum; PrimeSim HSPICE; PrimeSim SPICE); CADENCE (Spectre); SIEMENS (AFS); KEYSIGHT (Golden Gate); EMPYREAN (ALPS); MATHWORKS (Unknown)
	Schematic Design	Design Environment	34	[…]	SYNOPSYS (PrimeWave Design Environment); CADENCE (Virtuoso ADE Suite); SIEMENS (Solido Design Environment); KEYSIGHT (ADS); EMPYREAN (Aether); SIGASI (Unknown)
Back-end	Layout	Layout	35	[…]	SYNOPSYS (Custom Compiler; Laker Layout); CADENCE (Virtuoso Layout Editor); SIEMENS (Taner); KEYSIGHT (ADS); EMPYREAN (Aether); SIGASI (Unknown); SILVACO (Unknown)
		Electromagnetic Device Synthesis	36	[…]	ANSYS (Helic FSA; VeloceRF); CADENCE (EMX; EMX Designer); KEYSIGHT (Unknown); CEMWORKS (Unknown); LORENTZ (PeakView EMD); XPEEDIC (iModeler)
	Physical Design	Early Power Integrity Analysis	37	[…]	ANSYS (PrimeX); CADENCE (Virtuoso EAD); SIEMENS (mPower)
	Physical Verification & Sign-off	Equivalence Checking	38	[…]	SYNOPSYS (ESP); CADENCE (Custom Conformal)
		Physical Verification	39	[…]	SYNOPSYS (IC Validator); CADENCE (Pegasus); SIEMENS (Calibre); KEYSIGHT (Unknown); EMPYREAN (Argus); SILVACO (Unknown)
		ESD Analysis	40	[…]	SYNOPSYS (ICV PERC; PrimeESD); ANSYS (PathFinder (+SC)); CADENCE (PVS-PERC; Pegasus-PERC; Voltus ESD); SIEMENS (Calibre PERC); KEYSIGHT (Unknown); ANGSTROM DESIGN AUTOMATION (DECIMM); DASSAULT (CST Studio); MAGWEL (ESDi); SILVACO (Unknown)
		Transistor-level Power Integrity Analysis	41	[…]	SYNOPSYS (PrimeSim Reliability Analysis); ANSYS (Totem (+SC)); CADENCE (Voltus-Fi); SIEMENS (mPower); EMPYREAN (Patron); MATHWORKS (Unknown); SIGASI (Unknown)
		Power Device Analysis	42	[…]	SYNOPSYS (Power Device Workbench); ANSYS (PowerX); EMPYREAN (Polas); JEDAT (PowerVolt); MAGWEL (PTM); PRIMARIUS (PRM); SIGASI (Unknown)
		Electromagnetic Modelling	43	[…]	ANSYS (Electronics Enterprise; Electronics Pro; Helic FSA; RaptorH; RaptorQu; RaptorX); CADENCE (Clarity; EMX; EMX Planar 3D Solver); KEYSIGHT (Momentum; PathWave EM Design - EMPro; QuantumPro; RFPro); EMPYREAN (XModel; Xmodel); ALTIUM (Unknown); CEMWORKS (Unknown); LORENTZ (PeakView LEM); MATHWORKS (Unknown); XPEEDIC (IRIS; Metis); ZUKEN (Unknown)
		Electromagnetic Extraction	44	[…]	ANSYS (Electronics Enterprise; Exalto; Helic FSA; Q3D Extractor); CADENCE (Clarity; EMX; QRC; Quantus); SIEMENS (Calibre 3DSTACK; Calibre XRC; Calibre xACT);

Level 1	Level 2	Level 3	Segment ID	Market size (USD […])	List of tools
					KEYSIGHT (ADS; RFPro); CEMWORKS (Unknown); LORENTZ (PeakView HFD); MATHWORKS (Unknown)
		Parasitic Extraction	45	[…]	SYNOPSYS (F3D; Quick Cap; StarRC); CADENCE (Quantus Extraction; Quantus FS); SIEMENS (Calibre XACT 3D; Calibre xRC); EMPYREAN (Empyrean RCExplorer)
		Parasitic Analysis	46	[…]	SYNOPSYS (Pillar); ANSYS (ParagonX); CADENCE (I-DSPF; QRC; Quantus Smart View; Virtuoso EAD); SIEMENS (Calibre xRC); EMPYREAN (ADA); SIGASI (Unknown); SILVACO (Viso; edXact)
		Reliability Analysis	47	[…]	SYNOPSYS (P2P; PrimeSim Reliability Analysis); CADENCE (Legato Reliability); SIEMENS (Unknown)
		Thermal Analysis	48	[…]	SYNOPSYS (Ethan); CADENCE (Celsius); JEDAT (Thermal Analysis); MAGWEL (Thermal Analysis)
		Electromagnetic Simulation	49	[…]	ANSYS (Electronics Enterprise; HFSS (-IC)); CADENCE (Clarity; EMX); KEYSIGHT (PathWave EM Design - EMPro; RFPro); DASSAULT (CST Studio Suite)
	Post-Layout Simulation	Circuit Simulation	50	[…]	SYNOPSYS (PrimeSim Continuum; PrimeSim HSPICE; PrimeSim Pro; PrimeSim SPICE; PrimeSim XA); CADENCE (Spectre); MATHWORKS (Unknown)
		Design Environment	51	[…]	SYNOPSYS (WaveView); CADENCE (Virtuoso ADE Suite; Viva); SIEMENS (EasyWave); SIGASI (Unknown)

Source: Reply to RFI 19, Annex Q.3.1.

Table 4. Segments and tools in the Mixed-signal & Photonic Design Flows.

Level 0	Level 1	Level 2	Level 3	Segment ID	Market size (USD […])	List of tools
Mixed-signal Design Flow	Front end	Co-Simulation	Co-Simulation Enabling Kit	52	[…]	SYNOPSYS (VCS PrimeSim Co-Simulation); CADENCE (AMSDesigner); SIEMENS (Symphony)
	Back-end	Co-Design	Co-Design Enabling Kit	53	[…]	SYNOPSYS (Custom Compiler); CADENCE (Innovus; Virtuoso); SIGASI (Unknown); SILVACO (Unknown)
Photonic Design Flow	Front-end	Schematic Design	Photonic Layout Design Implementation	54	[…]	SYNOPSYS (OptoCompiler); CADENCE (Virtuoso; Virtuoso Photonic Platform); SIEMENS (L-edit); LATITUDE (PIC Studio); LUCEDA PHOTONICS (IPKISS); SIGASI (Unknown); SILVACO (Unknown); WIEWEB (CleWin)
		Pre-Layout Simulation	Photonic Chip Simulation	55	[…]	SYNOPSYS (OptSim); ANSYS (Lumerical Interconnect); CADENCE (Spectre); KEYSIGHT (Keysight Photonic Application Suite); DASSAULT (CST Studio Suite); IN-HOUSE SOLUTIONS (Unknown); OPTISYSTEM (OptiSPICE); OPTIWAVE (Unknown); PHOTON DESIGN (PIC Wave); SIGASI (Unknown); SILVACO (Unknown); VPI PHOTONICS (VIPItransmissionMaker; VPIcomponentMaker)
		Layout	Photonic Layout Design Implementation	56	[…]	SYNOPSYS (OptoCompiler); CADENCE (Virtuoso; Virtuoso Photonic Platform); SIEMENS (L-edit); LATITUDE (PIC Studio); LUCEDA PHOTONICS (IPKISS); SIGASI (Unknown); SILVACO (Unknown); WIEWEB (CleWin)
	Back-end	Post-Layout Simulation	Photonic Chip Simulation	57	[…]	ANSYS (Lumerical Interconnect); CADENCE (Spectre); KEYSIGHT (Keysight Photonic Application Suite); DASSAULT (CST Studio Suite); IN-HOUSE SOLUTIONS (Unknown); OPTISYSTEM (OptiSPICE); OPTIWAVE (Unknown); PHOTON DESIGN (PIC Wave); SIGASI (Unknown); SILVACO (Unknown); VPI PHOTONICS (VIPItransmissionMaker; VPIcomponentMaker)

Source: Reply to RFI 19, Annex Q.3.1.

Table 5. Tools used within the Multi-die Design Flow.

Level 1	Level 2	Level 3	Segment ID	Market size (USD […])	List of tools
Front-end	Pre-Layout Simulation	Circuit Simulation	58	[…]	SYNOPSYS (PrimeSim Continuum; PrimeSim HSPICE; PrimeSim SPICE); CADENCE (Spectre); SIEMENS (AFS); KEYSIGHT (Golden Gate); EMPYREAN (ALPS); MATHWORKS (Unknown)
	Architectural Design	Early Architectural Exploration	59	[…]	SYNOPSYS (Platform Architect); CADENCE (Interconnect Workbench); SIEMENS (Vista Flow); KEYSIGHT (Unknown); MATHWORKS (Unknown); ZUKEN (Unknown)
		Architectural Design & Implementation	60	[…]	SYNOPSYS (3DIC Compiler); CADENCE (APD; Integrity 3D-IC); SIEMENS (Innovator 3D-IC; xPedition)

Level 1	Level 2	Level 3	Segment ID	Market size (USD […])	List of tools
	Logic / Circuit Design	Static Verification	61	[…]	SYNOPSYS (VC SpyGlass); CADENCE (JasperLint); SIEMENS (Questa Lint/CDC); REAL INTENT (Ascent AutoFormal; Ascent Lint; Meridian CDC; Meridian RDC)
		Silicon Lifecycle Management IP	62	[…]	SYNOPSYS (Synopsys SLM CDM IP; Synopsys SLM HSAT IP; Synopsys SLM PMM IP; Synopsys SLM PVT IP; Synopsys SLM XLBIST IP); SIEMENS (Tessent Embedded Analytics); PROTEANTECS (Agents)
		Design-for-Test / Test IP	63	[…]	SYNOPSYS (Synopsys SLM SHS IP; Synopsys SLM SMS IP; TestMAX Access; TestMAX Advisor; TestMAX DFT; TestMAX LBIST Add-on; TestMAX Manager; TestMAX SMS); CADENCE (Modus); SIEMENS (Tessent); SYNTEST (DFT-PRO; TurboBIST; TurboSCAN)
	Functional Verification	Simulation Verification	64	[…]	SYNOPSYS (VCS; VSO.ai; Z01X); CADENCE (Xcelium); SIEMENS (Questa)
		Debug Verification	65	[…]	SYNOPSYS (Euclide; VC Execution Manager; Verdi); CADENCE (Verisium (aka Indago)); SIEMENS (Questa Visualizer)
		Formal Verification	66	[…]	SYNOPSYS (VC Formal); CADENCE (JasperGold); SIEMENS (Questa Formal & OneSpin); VENNSA (Unknown)
		Hardware-Assisted Verification	67	[…]	SYNOPSYS (HAPS; ZeBu); CADENCE (Palladium/Protium); SIEMENS (Veloce CS)
		Static Verification	68	[…]	SYNOPSYS (VC SpyGlass); CADENCE (JasperLint); SIEMENS (Questa Lint/CDC); REAL INTENT (Ascent AutoFormal; Ascent Lint; Meridian CDC; Meridian RDC)
Back-end	Physical Verification & Sign-off	Physical Verification	69	[…]	SYNOPSYS (IC Validator); CADENCE (Pegasus); SIEMENS (Calibre); KEYSIGHT (Unknown); EMPYREAN (Argus); SILVACO (Unknown)
		ESD Analysis	70	[…]	SYNOPSYS (ICV PERC; PrimeESD); ANSYS (PathFinder (+SC)); CADENCE (Pegasus-PERC; Voltus ESD); SIEMENS (Calibre PERC); KEYSIGHT (Unknown); ANGSTROM DESIGN AUTOMATION (DECIMM); DASSAULT (CST Studio); MAGWEL (ESDi); SILVACO (Unknown)
		Timing Analysis	71	[…]	SYNOPSYS (PrimeTime); CADENCE (Tempus); SIEMENS (Unknown)
		Transistor-level Power Integrity Analysis	72	[…]	SYNOPSYS (PrimeSim Reliability Analysis); ANSYS (Totem (+SC)); CADENCE (Voltus-Fi); SIEMENS (mPower); EMPYREAN (Patron); MATHWORKS (Unknown); SIGASI (Unknown)
		Parasitic Extraction	73	[…]	SYNOPSYS (StarRC); CADENCE (Quantus Extraction); SIEMENS (Calibre xRC); EMPYREAN (Empyrean RCExplorer)
		Reliability Analysis	74	[…]	SYNOPSYS (PrimeSim Reliability Analysis); CADENCE (Legato Reliability); SIEMENS (Unknown)
		Structural and Thermal Analysis	75	[…]	ANSYS (Electronics Enterprise; Icepak; RedHawk-SC Electrothermal); CADENCE (Celsius; Integrity 3D-IC); SIEMENS (Calibre 3DThermal; Flotherm XT); KEYSIGHT (PathWave Thermal Design); ALTAIR (ElectroFlo); ALTIUM (Unknown); CEMWORKS (Unknown); COSMOL (Heat Transfer Module); MATHWORKS (Unknown); ZUKEN (Unknown)
		Signal and Power Integrity	76	[…]	ANSYS (Electronics Enterprise; HFSS (-IC); Helic FSA; Q3D Extractor; RaptorH; RaptorQu; RaptorX; RedHawk (+SC); RedHawk-SC Electrothermal; SIwave); CADENCE (Clarity; EMX 3D Planar; Integrity 3D-IC; Sigrity; Voltus-Fi); SIEMENS (HyperLynx); KEYSIGHT (Momentum); EMPYREAN (Patron); ALTIUM (Unknown); CEMWORKS (Unknown); LORENTZ (PeakView LEM); MATHWORKS (Unknown); ZUKEN (Unknown)

Level 1	Level 2	Level 3	Segment ID	Market size (USD […])	List of tools
	Post-Layout Simulation	Circuit Simulation	77	[…]	SYNOPSYS (PrimeSim Continuum; PrimeSim HSPICE; PrimeSim Pro; PrimeSim SPICE; PrimeSim XA); CADENCE (Spectre); MATHWORKS (Unknown)

Source: Reply to RFI 19, Annex Q.3.1.

Table 6. Segments and tools in the PCB and Packaging Design flows and Outside EDA Design Flows.

Level 0/1	Level 2	Level 3	Segment ID	Market size (USD […])	List of tools
Back-end	Verification	PCB Analysis	79	[…]	ANSYS (Electronics Enterprise; Electronics Pro; HFSS (-IC); Icepak; Maxwell; Q3D Extractor; SIwave); CADENCE (Sigrity, Celsius PowerDC, Clarity 3D Solver); SIEMENS (HyperLynx, Xpedition, Calibre3D Thermal, Simcenter Flotherm); KEYSIGHT (ADS); ALTIUM (Altium Designer, PDN Analyzer); ZUKEN (CR-8000)
Packaging Design Flow	Verification	Packaging	80	[…]	ANSYS (Electronics Enterprise; Electronics Pro; HFSS (-IC); Icepak; Maxwell; Q3D Extractor; SIwave); CADENCE (Allegro, Sigrity, Clarity 3D Solver, Celsius PowerDC); SIEMENS (Xpedition, HyperLynx, Calibre3D Thermal, Simcenter Flotherm); KEYSIGHT (ADS); ALTIUM (Altium Designer); ZUKEN (CR-8000)
Outside of Design Flow	Outside of Design Flow	Characterization	81	[…]	SYNOPSYS (NanoTime; PrimeLib; SiliconSmart); CADENCE (Liberate); SIEMENS (Solido); EMPYREAN (Liberal); SILVACO (Library Platform (Cielo, Viola))
		Functional Safety & Specification Analysis	82	[…]	SYNOPSYS (VC Functional Safety Manager); ANSYS (Medini Analyze for Semiconductors); CADENCE (Midas; Midas Platform); SIEMENS (Austemper); APIS (FTA; IQ-FMEA); C2A / VULTARA / ITEMIS (Cybersecurity analysis); ENCO SAFETY OFFICE (SoX); IN-HOUSE SOLUTIONS (N/A); ISOGRAPH (Reliability Workbench); PLATO (e1ns FMEA); VECTOR (PREEVision Safety Extension)
		Mask Tools	84	[…]	SYNOPSYS (CATS; IC Validator; Proteus; S-Litho; Silicon Workbench); CADENCE (PPC); SIEMENS (Calibre); ASML (ASL Computational Lithography)
		TCAD	86	[…]	SYNOPSYS (QuantumATK; Raphael; Sentaurus Calibration Workbench; Sentaurus Customer Product; Sentaurus Device; Sentaurus Interconnect; Sentaurus Parallel; Sentaurus Process; Sentaurus Process Explorer; Sentaurus Structure Editor; Sentaurus Topography; Sentaurus Visual; Sentaurus Workbench; Simpleware AS Cardio; Simpleware Academic; Simpleware Apex; Simpleware Base; Simpleware CAD; Simpleware CAD Academic; Simpleware Elite; Simpleware ScanIP; TCAD to SPICE; Taurus Device; Taurus Medici; Taurus TSumprem4); LAM (Coventor); SILVACO (Utmost; Victory)
		Virtual Prototyping	87	[…]	SYNOPSYS (Silver; Virtualizer); CADENCE (Helium); SIEMENS (Hycon); MATHWORKS (Unknown)

Source: Reply to RFI 19, Annex Q.3.1.
Segment ID 88 groups legacy products of the Parties and is omitted.

Table 7. Offerings and Segments in Design IP.

Level 1/2	Level 3	Segment ID	Market size (USD […])	Design IP offers
Design IP	Embedded Memories	89	[…]	Synopsys Memory Compilers; ARM (Arm Artisan); M31 (M31 Memory Compiler); OTHERS (Others)
	NVM Other Memory Compilers	90	[…]	Synopsys Non-Volatile Memories; EMEMORY (NeoFuse, NeoBit, NeoEE, NeoMTP, NeoFlash); NSCORE (Others); OTHERS (Others); SST (SuperFlash)
	Physical Libraries	91	[…]	Synopsys Physical Libraries; ARAGIO (Aragio I/O Library IP); ARM (Artisan); OTHERS (Others); VERISILICON (V.Libs)
	Wired Interface IP	92	[…]	Synopsys Wired Interface IP Family; Cadence Protocol IP; ALPHAWAVE (PHY IP); OTHERS (Others); RAMBUS (Rambus Interconnect IP)
	Wireless Interface IP	93	[…]	Synopsys Wireless Interface IP Family; ACTT (ACTT Interface IP); CEVA (Ceva-Waves); MINDTREE (BlueLit, BlueWix, EtherMind); OTHERS (Others)
	Security IP	94	[…]	Synopsys Security IP implementing cryptographic functions, Physical Unclonable Function; ARM (TrustZone, SecurCore, Cortex-M35P); OTHERS (Others); RAMBUS (Rambus Security IP portfolio); SECURE IC (Security Silicon IP)
	CPU IP	95	[…]	Synopsys ARC Processor IP Family; ANDES (AndesCore); ARM (Cortex, Neoverse); IMAGINATION (Catapult); OTHERS (Others); SIFIVE (SiFive Core IP)
	DSP IP	96	[…]	Synopsys ARC DSP, ARC VPX DSP; Cadence Tensilica; CEVA (SensPro, BX); OTHERS (Others); VERISILICON (ZSP)
	Other Excl Security IP	97	[…]	Synopsys Other IP products; ARM (Arm Other IP products); ARTERISIP (Arteris Other IP products); OTHERS (Others); VERISILICON (Verisilicon Other IP products)

Source: Reply to RFI 19, Annex Q.3.1.

3.2 Product mapping – functional level (Functional ID level)

(29) As discussed in Section 4.2.1.3 of the Decision, the Commission concludes that it is appropriate to segment the EDA markets at the level of EDA functions. This has also been confirmed by the Product mapping exercise:

(30) **First,** in addition to the Parties, some market participants were also asked to map EDA tools to EDA design flow combinations. Their replies to the Commission's Requests for Information revealed that market participants have slightly diverging views on market segmentation and the presence of tools in different market segments.

(31) **Second,** the Notifying Party was asked to reconcile these differences where they had an impact on the competitive assessment.[24] In that regard, the Notifying Party argues that there exists no universally agreed segmentation within EDA and that the product mapping provided by the Parties would reflect their best efforts to capture demand-side substitutability at the functional level (i.e. level 3) and would best capture competitive dynamics for purposes of a substantive assessment of the Transactions' competitive impact. It would also be consistent with how the Parties analyse the relevant segments in their internal documents.[25]

(32) The segmentation at the functional level is therefore the most objective way to segment EDA markets and is in line with demand-side substitutability.[26]

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24 RFI 18, Q1.

25 Reply to RFI 18, para 1.1.

26 Decision, Section 4.2.1.3.

(33) At the functional level, there are **59 EDA functions** uniquely identified at L3 level and indexed by a unique **Functional ID**.[27] This segmentation reflects all possible EDA functions, irrespective of whether the same EDA function appears in more than one design flow and/or design stage.[28] Including Design IP segments, there is a total of 68 EDA functions/Design IP segments.

(34) **Table 8** lists all EDA functions and Design IP segments identified by the Parties and indicates where EDA functions appear in multiple design flows and or design stages.

Table 8. EDA functions and Design IP segments..

Functional IDs	Associated Segment IDs	EDA function or Design IP segment (Level 3)	Market size (USD […], 2023)
		EDA functions	[…]
1	1	High-Level Synthesis	[…]
2	2	RTL Analysis	[…]
3	3	RTL Power Consumption Analysis	[…]
4	4; 59	Early Architectural Exploration	[…]
5	5	RTL Synthesis	[…]
6	6	FPGA Synthesis	[…]
7	7; 15; 61; 68	Static Verification	[…]
8	8	Gate-level Power Consumption Analysis	[…]
9	9; 19	Timing Constraints	[…]
10	10; 62	Silicon Lifecycle Management IP	[…]
11	11; 63	Design-for-Test / Test IP	[…]
12	12; 64	Simulation Verification	[…]
13	13; 65	Debug Verification	[…]
14	14; 66	Formal Verification	[…]
16	16	Emulation-Based Power Analysis	[…]
17	17; 67	Hardware-Assisted Verification	[…]
18	18	Place & Route	[…]
20	20; 38	Equivalence Checking	[…]
21	21; 39; 69	Physical Verification	[…]
22	22; 40; 70	ESD Analysis	[…]
23	23; 71	Timing Analysis	[…]
24	24	ECO	[…]
25	25	Clock Jitter Analysis	[…]
26	26; 43	Electromagnetic Modelling	[…]
27	27; 45; 73	Parasitic Extraction	[…]
28	28; 46	Parasitic Analysis	[…]
29	29	Design Robustness	[…]
30	30	Gate-level Power Integrity Analysis	[…]
31	31	Gate-level Security Analysis	[…]
32	32	Schematic Editing	[…]
33	33; 50; 58; 77	Circuit Simulation	[…]
34	34; 51	Design Environment	[…]
35	35	Layout	[…]
36	36	Electromagnetic Device Synthesis	[…]
37	37	Early Power Integrity Analysis	[…]
41	41; 72	Transistor-level Power Integrity Analysis	[…]
42	42	Power Device Analysis	[…]
44	44	Electromagnetic Extraction	[…]
47	47; 74	Reliability Analysis	[…]
48	48	Thermal Analysis	[…]
49	49	Electromagnetic Simulation	[…]

[27] The Functional ID is defined as the minimum of Segment IDs with the same function. For example, "Circuit Simulation" appears twice in the Analog Flow and twice in the Multi-die Flow in stages Pre-Layout Simulation and Post-Layout Simulation, Segment IDs 33, 50, 58 and 77, and therefore is assigned Functional ID 33.

[28] EDA functions are defined broadly, including the photonic design flow, PCB and packaging design and EDA tools outside design flows. In addition, the product mapping also includes Design IP. There are 9 Design IP segments. Including Design IP, there is a total of 68 Functional IDs and 97 Segment IDs.

Functional IDs	Associated Segment IDs	EDA function or Design IP segment (Level 3)	Market size (USD […], 2023)
52	52	Co-Simulation Enabling Kit	[…]
53	53	Co-Design Enabling Kit	[…]
54	54; 56	Photonic Layout Design Implementation	[…]
55	55; 57	Photonic Chip Simulation	[…]
60	60	Architectural Design & Implementation	[…]
75	75	Structural and Thermal Analysis	[…]
76	76	Signal and Power Integrity	[…]
78	78	PCB Design	[…]
79	79	PCB Analysis	[…]
80	80	Packaging	[…]
81	81	Characterization	[…]
82	82	Functional Safety & Specification Analysis	[…]
83	83	HAT	[…]
84	84	Mask Tools	[…]
85	85	Synthesis	[…]
86	86	TCAD	[…]
87	87	Virtual Prototyping	[…]
88	88	N/A	[…]
		Design IP segments	[…]
89	89	Embedded Memories	[…]
90	90	NVM Other Memory Compilers	[…]
91	91	Physical Libraries	[…]
92	92	Wired Interface IP	[…]
93	93	Wireless Interface IP	[…]
94	94	Security IP	[…]
95	95	CPU IP	[…]
96	96	DSP IP	[…]
97	97	Other Excl Security IP	[…]

Source: Reply to RFI 19, Annex Q.3.1, Commission assessment.

3.3 Revenue and market size data

(35) The following subsections describe the Parties' methodology with regard to the allocation of (i) revenues for their own products, (ii) best estimates of segment sizes, (iii) best estimates of rivals' revenues, as well as (iv) granular information on interoperability flows between functions.[29]

3.3.1 The Parties' revenues for their own products

(36) Synopsys provided its internal revenue estimates based on its own internal market intelligence tracking data, [Synopsys' market intelligence].[30]

(37) Ansys explained that [information on Ansys revenue allocation].[31]

(38) The Parties excluded excel/homegrown solutions from their merchant market shares, with the exception of the internal best estimates provided for the functional safety specification and analysis category in the Draft Form CO.

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29 The Parties product mapping exercise is explained in Form CO, Chapter 2 – Annex 11.2 Methodology note accompanying the product and revenue mapping template. The latest versions of the product mapping and EDA functional shares were submitted in the Form CO, Chapter 2, Annex RFI 19 Q.3.1 and Annex RFI 18 Q.4.1 respectively.

30 Based on Synopsys's internal view of [Synopsys' market intelligence] data, which [description of Synopsys revenue allocation].

31 Based on Ansys's [information on Ansys revenue allocation], which allocates revenue over contract duration for subscriptions.

(39) The Parties' products often have applications in multiple segments, making it difficult to determine the exact proportion of revenue attributed to each segment. To address this, the Parties provided their best estimates of the proportion of revenues to be attributed to each segment. These estimates were based on 2023 data and focused on the primary functionalities driving customer demand. To account for overlapping product applicability, the Parties' revenues were calculated by multiplying the product's total revenue by the Parties' estimates of what proportion of their revenues should be allocated to each product segment.

3.3.2 The Parties' best estimates of segment sizes

(40) The Parties estimated segment sizes per design flow combinations using a "top-down" approach, starting with Synopsys's [Synopsys' market intelligence] data.[32]

(41) Synopsys uses data from ESDA[33] as the starting point for its assessment of EDA market shares. As indicated above, this is the only third-party data source publishing actual revenue data on detailed EDA product categories.

(42) The Parties noted that not all EDA suppliers report revenues to ESDA and therefore not all relevant revenues are included in ESDA's published market totals. Synopsys believes that around [80-90]% of relevant revenues for each ESDA category are captured by ESDA, and that this therefore provides an acceptable market representation. If fewer than three companies report data to ESDA for a certain product category, ESDA does not provide revenue figures for this category. Instead, multiple (often related) categories will be grouped and more aggregate data will be published by ESDA.[4]

(43) The Parties indicated that [Synopsys' estimated data segments] are generally aligned with ESDA product categories, [Synopsys' market intelligence]. The Parties provided their best estimates of how to divide each [estimated] segment size across the relevant flow level combinations. The Parties applied the same approach for estimating the segment sizes for categories falling outside of the EDA design flow, where applicable.

3.3.3 The Parties' best estimates of rivals' revenues

(44) The Parties used their best efforts to identify rivals for the design flow combinations in which either Party is active. Where possible, the Parties also identified the names of rival products.

(45) [The Parties' market intelligence practice]. The Parties, therefore, estimated their rivals' revenues based on their general understanding of the industry, their internal know-how and market intelligence.

(46) To estimate competitor revenues, a "top-down" approach was taken by allocating competitors' revenues in each [estimated] segment across associated functions and rescaling to match the remaining market sizes, accounting for the Parties' own sales.

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32 The Parties applied the same approach for estimating segment sizes for categories falling outside of the EDA design flow, where applicable.

33 ESDA is an independent third-party organization that collects information from its members in the EDA space. ESDA, established in 1987 by EDA companies, estimates total market revenues per quarter across a number of product categories primarily relating to Synopsys' EDA Group (EDAG), Solutions Group (SG) and Systems Design Group (SDG) products.

This initial estimate was then reviewed and adjusted by the Parties to better reflect commercial reality, with Synopsys assuming zero revenues for unreported rivals, and Ansys estimating shares based on internal know-how and market intelligence.

(47) During its investigation, the Commission requested revenue data from market participants other than the Parties to verify the Parties' best estimates. This exercise suggests that the Parties' best estimates provide a good approximation of the EDA market at the functional level and are the best attainable market share estimates at the design-flow combination level.

3.4 Market shares at the functional level (Functional ID level)

(48) Table 9 shows the market shares of the Parties', Siemens and Cadence, based on the Parties' estimates. Furthermore, the first column indicates which Segment IDs belong to each functional level, while the last columns indicate whether the functional level is horizontally or non-horizontally affected as well as the number of interoperability links (separately for the exporting and importing side).

Table 9. Market shares segmented according to the functional (L3) level.

Functional-level IDs	Segment IDs	Level 3	Market size (USD […])	Market shares (2023)					Aff. horizontally	Aff. non-horizontally	No. interoperability links	
				SNPS	ANSS	CDNS	SIE	Others			Exporting	Importing
1	1	High-Level Synthesis	[…]	[0-5]%	[0-5]%	[90-100]%	[5-10]%	[0-5]%				
2	2	RTL Analysis	[…]	[90-100]%	[0-5]%	[0-5]%	[0-5]%	[0-5]%		Yes	1	
3	3	RTL Power Consumption Analysis	[…]	[30-40]%	[40-50]%	[10-20]%	[10-20]%	[0-5]%	Yes	Yes	2	5
4	4; 59	Early Architectural Exploration	[…]	[5-10]%	[0-5]%	[10-20]%	[5-10]%	[70-80]%				
5	5	RTL Synthesis	[…]	[60-70]%	[0-5]%	[30-40]%	[0-5]%	[0-5]%		Yes	1	
6	6	FPGA Synthesis	[…]	[50-60]%	[0-5]%	[0-5]%	[10-20]%	[20-30]%		Yes		
7	7; 15; 61; 68	Static Verification	[…]	[60-70]%	[0-5]%	[0-5]%	[5-10]%	[10-20]%		Yes		
8	8	Gate-level Power Consumption Analysis	[…]	[70-80]%	[0-5]%	[20-30]%	[0-5]%	[0-5]%		Yes	1	2
9	9; 19	Timing Constraints	[…]	[40-50]%	[0-5]%	[20-30]%	[0-5]%	[20-30]%		Yes		
10	10; 62	Silicon Lifecycle Management IP	[…]	[50-60]%	[0-5]%	[0-5]%	[10-20]%	[30-40]%		Yes		
11	11; 63	Design-for-Test / Test IP	[…]	[30-40]%	[0-5]%	[10-20]%	[40-50]%	[5-10]%		Yes		
12	12; 64	Simulation Verification	[…]	[30-40]%	[0-5]%	[30-40]%	[20-30]%	[5-10]%		Yes	3	1
13	13; 65	Debug Verification	[…]	[70-80]%	[0-5]%	[10-20]%	[10-20]%	[0-5]%		Yes		1
14	14; 66	Formal Verification	[…]	[10-20]%	[0-5]%	[60-70]%	[10-20]%	[0-5]%				
16	16	Emulation-Based Power Analysis	[…]	[20-30]%	[0-5]%	[80-90]%	[0-5]%	[0-5]%		NB†	1	
17	17; 67	Hardware-Assisted Verification	[…]	[40-50]%	[0-5]%	[40-50]%	[10-20]%	[0-5]%		Yes	1	
18	18	Place & Route	[…]	[40-50]%	[0-5]%	[50-60]%	[0-5]%	[0-5]%		Yes	4	
20	20; 38	Equivalence Checking	[…]	[30-40]%	[0-5]%	50-60]%	[0-5]%	[0-5]%		Yes		
21	21; 39; 69	Physical Verification	[…]	[10-20]%	[0-5]%	[10-20]%	[60-70]%	[0-5]%				
22	22; 40; 70	ESD Analysis	[…]	[10-20]%	[10-20]%	[5-10]%	[60-70]%	[0-5]%	No**	Yes		5
23	23; 71	Timing Analysis	[…]	[80-90]%	[0-5]%	[5-10]%	[0-5]%	[0-5]%		Yes	2	2
24	24	ECO	[…]	[80-90]%	[0-5]%	[10-20]%	[0-5]%	[5-10]%		Yes	1	1
25	25	Clock Jitter Analysis	[…]	[0-5]%	[30-40]%	[30-40]%	[30-40]%	[0-5]%		Yes		8

Functional-level IDs	Segment IDs	Level 3	Market size (USD […])	Market shares (2023)					Aff. horizontally	Aff. non-horizontally	No. interoperability links	
				SNPS	ANSS	CDNS	SIE	Others			Exporting	Importing
26	26; 43	Electromagnetic Modelling	[…]	[0-5]%	[10-20]%	[20-30]%	[0-5]%	[60-70]%		NB†	1	3
27	27; 45; 73	Parasitic Extraction	[…]	[40-50]%	[0-5]%	[40-50]%	[0-5]%	[0-5]%		Yes	9	
28	28; 46	Parasitic Analysis	[…]	[0-5]%	[70-80]%	[10-20]%	[10-20]%	[0-5]%	Yes	Yes		5
29	29	Design Robustness	[…]	[70-80]%	[0-5]%	[10-20]%	[5-10]%	[0-5]%		Yes	2	
30	30	Gate-level Power Integrity Analysis	[…]	[0-5]%	[50-60]%	[30-40]%	[5-10]%	[0-5]%		Yes	3	14
31	31	Gate-level Security Analysis	[…]	[0-5]%	[90-100]%	[0-5]%	[0-5]%	[0-5]%		Yes	1	11
32	32	Schematic Editing	[…]	[5-10]%	[0-5]%	[80-90]%	[0-5]%	[0-5]%				
33	33; 50; 58; 77	Circuit Simulation	[…]	[30-40]%	[0-5]%	[30-40]%	[5-10]%	[20-30]%		Yes	4	9
34	34; 51	Design Environment	[…]	[10-20]%	[0-5]%	[80-90]%	[0-5]%	[0-5]%		NB†	1	1
35	35	Layout	[…]	[10-20]%	[0-5]%	[80-90]%	[0-5]%	[0-5]%		Yes	4	3
36	36	Electromagnetic Device Synthesis	[…]	[0-5]%	[10-20]%	[40-50]%	[0-5]%	[30-40]%		NB†	1	3
37	37	Early Power Integrity Analysis	[…]	[0-5]%	[0-5]%	[70-80]%	[10-20]%	[0-5]%		NB†		4
41	41; 72	Transistor-level Power Integrity Analysis	[…]	[0-5]%	[40-50]%	[40-50]%	[5-10]%	[5-10]%	Yes	Yes	3	6
42	42	Power Device Analysis	[…]	[40-50]%	[5-10]%	[0-5]%	[0-5]%	[50-60]%	Yes	Yes		6
44	44	Electromagnetic Extraction	[…]	[0-5]%	[5-10]%	[90-100]%	[0-5]%	[0-5]%		NB†	1	4
47	47; 74	Reliability Analysis	[…]	[20-30]%	[0-5]%	[0-5]%	[70-80]%	[0-5]%				
48	48	Thermal Analysis	[…]	[0-5]%	[0-5]%	[40-50]%	[0-5]%	[40-50]%				
49	49	Electromagnetic Simulation	[…]	[0-5]%	[50-60]%	[30-40]%	[0-5]%	[20-30]%		Yes	2	2
52	52	Co-Simulation Enabling Kit	[…]	[20-30]%	[0-5]%	[40-50]%	[20-30]%	[0-5]%				
53	53	Co-Design Enabling Kit	[…]	[5-10]%	[0-5]%	[90-100]%	[0-5]%	[0-5]%		NB†	1	
54	54; 56	Photonic Layout Design Implementation	[…]	[20-30]%	[0-5]%	[30-40]%	[0-5]%	[30-40]%		NB†	1	
55	55; 57	Photonic Chip Simulation	[…]	[10-20]%	[10-20]%	[30-40]%	[5-10]%	[30-40]%	Yes	Yes	1	
60	60	Architectural Design & Implementation	[…]	[20-30]%	[0-5]%	[40-50]%	[20-30]%	[0-5]%		NB†	3	2
75	75	Structural and Thermal Analysis	[…]	[0-5]%	[70-80]%	[20-30]%	[10-20]%	[0-5]%	Yes*	Yes	3	1
76	76	Signal and Power Integrity	[…]	[0-5]%	[30-40]%	[40-50]%	[0-5]%	[10-20]%	Yes*	Yes	1	1
78	78	PCB Design	[…]	[0-5]%	[0-5]%	[10-20]%	[50-60]%	[20-30]%				
79	79	PCB Analysis	[…]	[0-5]%	[10-20]%	[10-20]%	[40-50]%	[20-30]%		NB†	1	1
80	80	Packaging	[…]	[0-5]%	[10-20]%	[10-20]%	[40-50]%	[20-30]%		NB†	1	1
81	81	Characterization	[…]	[40-50]%	[0-5]%	[40-50]%	[10-20]%	[0-5]%		Yes	4	
82	82	Functional Safety & Specification Analysis	[…]	[10-20]%	[10-20]%	[40-50]%	[20-30]%	[10-20]%	Yes	NB†	5	
83	83	HAT	[…]	[90-100]%	[0-5]%	[0-5]%	[10-20]%	[0-5]%		Yes		
84	84	Mask Tools	[…]	[20-30]%	[0-5]%	[0-5]%	[40-50]%	[20-30]%				
85	85	Synthesis	[…]	[30-40]%	[0-5]%	[60-70]%	[0-5]%	[0-5]%		Yes		
86	86	TCAD	[…]	[80-90]%	[0-5]%	[0-5]%	[0-5]%	[20-30]%		Yes		
87	87	Virtual Prototyping	[…]	[80-90]%	[0-5]%	[5-10]%	[0-5]%	[0-5]%		Yes		
89	89	Embedded Memories	[…]	[50-60]%	[0-5]%	[0-5]%	[0-5]%	[40-50]%		Yes	10	
90	90	NVM Other Memory Compilers	[…]	[10-20]%	[0-5]%	[0-5]%	[0-5]%	[80-90]%		NB†	5	

Functional-level IDs	Segment IDs	Level 3	Market size (USD […])	Market shares (2023)					Aff. horizontally	Aff. non-horizontally	No. interoperability links	
				SNPS	ANSS	CDNS	SIE	Others			Exporting	Importing
91	91	Physical Libraries	[…]	[30-40]%	[0-5]%	[0-5]%	[0-5]%	[60-70]%		Yes	10	
92	92	Wired Interface IP	[…]	[60-70]%	[0-5]%	[10-20]%	[0-5]%	[20-30]%		Yes	6	
93	93	Wireless Interface IP	[…]	[0-5]%	[0-5]%	[0-5]%	[0-5]%	[0-5]%		NB†	1	
94	94	Security IP	[…]	[10-20]%	[0-5]%	[0-5]%	[0-5]%	[80-90]%				
95	95	CPU IP	[…]	[0-5]%	[0-5]%	[0-5]%	[0-5]%	[90-100]%				
96	96	DSP IP	[…]	[0-5]%	[0-5]%	[60-70]%	[0-5]%	[30-40]%				
97	97	Other Excl Security IP	[…]	[0-5]%	[0-5]%	[0-5]%	[0-5]%	[90-100]%				

*Source: Reply to RFI 19, Annex Q.3.1. Reply to RFI 18, Annex Q.4.1. SNPS is Synopsys, ANSS is Ansys, CDNS is Cadence, SIE is Siemens. *Affected due to potential competition concerns. **While not horizontally affected, the Commission has assessed the impact of the Transaction due to concerns raised by market participants, see Decision, Section 5.2.3.1. †Neighbouring market with interoperability links to other EDA markets where the Parties have market shares of 30% or above.*

(49) To sum up, the Parties are active in a large number of EDA and Design IP markets, many of which are affected due to actual or potential overlaps or give rise to conglomerate links, listed in Section 5.2.3 and Section 5.2.4 of the Decision.

4 INTEROPERABILITY MATRIX (EDA AND DESIGN IP)

4.1 Interoperability relationships between EDA and Design IP

(50) The Commission requested the Parties to complete a matrix identifying data export-import relationships between EDA tools at a granular level for each segment ID where one or both of the Parties generated revenues in 2023. That is, the abovementioned market segments may be preceding or succeeding other segments market in the design flow – *i.e.*, one product exports data and information then imported by another product.

(51) Table 10 shows the export-import relationships across Segment IDs for each functional level (L3). This table also shows which relationships are affected from a conglomerate perspective at the functional level. That is, whether the Parties' combined market share in either the exporting or importing function is at least 30%, or whether one of the Parties' market share in either the exporting (or importing) function is at least 30% and the other Party is present in the importing (or exporting) function. There are in total 102 import-export relationships non-horizontally affected at the functional level.

Table 10. Overview of interoperability links at the functional level.

Exporting functional level IDs	Exporting function (L3)	Full list of Exporting Segment IDs	Importing functional level IDs	Importing function (L3)	Full list of Importing Segment IDs	Affected non-horizontally
2	RTL Analysis	3; 5; 8; 12; 15; 20	3	RTL Power Consumption Analysis	2; 12; 17; 81; 82	Yes
			5	RTL Synthesis	2; 7; 9; 10; 11; 19; 62; 63; 92; 93; 94; 95; 96; 97	
			7	Static Verification	2; 5; 18	
			8	Gate-level Power Consumption Analysis	2; 3; 5; 12; 16; 27; 82	
			12	Simulation Verification	2; 5; 6; 7; 15; 18; 23; 31; 52; 61; 68	
			20	Equivalence Checking	2; 5; 18	
3	RTL Power Consumption Analysis	8; 30	8	Gate-level Power Consumption Analysis	2; 3; 5; 12; 16; 27; 82	Yes
			30	Gate-level Power Integrity Analysis	3; 8; 12; 16; 18; 23; 24; 27; 29; 81; 82; 89; 90; 91	Yes
5	RTL Synthesis	8; 12; 15; 18; 20; 31	7	Static Verification	2; 5; 18	
			8	Gate-level Power Consumption Analysis	2; 3; 5; 12; 16; 27; 82	
			12	Simulation Verification	2; 5; 6; 7; 15; 18; 23; 31; 52; 61; 68	
			18	Place & Route	5; 8; 9; 15; 19; 21; 24; 53; 60; 92; 93; 94; 95; 96; 97	
			20	Equivalence Checking	2; 5; 18	
			31	Gate-level Security Analysis	5; 12; 18; 23; 27; 29; 81; 82; 89; 90; 91	Yes
6	FPGA Synthesis	12; 13	12	Simulation Verification	2; 5; 6; 7; 15; 18; 23; 31; 52; 61; 68	
			13	Debug Verification	6; 7; 12; 14; 15; 17; 52; 61; 64; 66; 67; 68; 82	
7	Static Verification	5; 12; 13; 18; 64; 65	5	RTL Synthesis	2; 7; 9; 10; 11; 19; 62; 63; 92; 93; 94; 95; 96; 97	
			12	Simulation Verification	2; 5; 6; 7; 15; 18; 23; 31; 52; 61; 68	
			13	Debug Verification	6; 7; 12; 14; 15; 17; 52; 61; 64; 66; 67; 68; 82	
			18	Place & Route	5; 8; 9; 15; 19; 21; 24; 53; 60; 92; 93; 94; 95; 96; 97	
8	Gate-level Power Consumption Analysis	18; 30	18	Place & Route	5; 8; 9; 15; 19; 21; 24; 53; 60; 92; 93; 94; 95; 96; 97	
			30	Gate-level Power Integrity Analysis	3; 8; 12; 16; 18; 23; 24; 27; 29; 81; 82; 89; 90; 91	Yes
9	Timing Constraints	5; 18; 23	5	RTL Synthesis	2; 7; 9; 10; 11; 19; 62; 63; 92; 93; 94; 95; 96; 97	
			18	Place & Route	5; 8; 9; 15; 19; 21; 24; 53; 60; 92; 93; 94; 95; 96; 97	
			23	Timing Analysis	9; 18; 19; 24; 27; 30; 60; 75; 81; 92; 93; 94; 95; 96; 97	
10	Silicon Lifecycle Management IP	2; 5	2	RTL Analysis	10; 62	
			5	RTL Synthesis	2; 7; 9; 10; 11; 19; 62; 63; 92; 93; 94; 95; 96; 97	
11	Design-for-Test / Test IP	5	5	RTL Synthesis	2; 7; 9; 10; 11; 19; 62; 63; 92; 93; 94; 95; 96; 97	

Exporting functional level IDs	Exporting function (L3)	Full list of Exporting Segment IDs	Importing functional level IDs	Importing function (L3)	Full list of Importing Segment IDs	Affected non-horizontally
12	Simulation Verification	3; 8; 13; 30; 31; 65	3	RTL Power Consumption Analysis	2; 12; 17; 81; 82	Yes
			8	Gate-level Power Consumption Analysis	2; 3; 5; 12; 16; 27; 82	
			13	Debug Verification	6; 7; 12; 14; 15; 17; 52; 61; 64; 66; 67; 68; 82	
			30	Gate-level Power Integrity Analysis	3; 8; 12; 16; 18; 23; 24; 27; 29; 81; 82; 89; 90; 91	Yes
			31	Gate-level Security Analysis	5; 12; 18; 23; 27; 29; 81; 82; 89; 90; 91	Yes
14	Formal Verification	13; 65	13	Debug Verification	6; 7; 12; 14; 15; 17; 52; 61; 64; 66; 67; 68; 82	
16	Emulation-Based Power Analysis	8; 30	8	Gate-level Power Consumption Analysis	2; 3; 5; 12; 16; 27; 82	
			30	Gate-level Power Integrity Analysis	3; 8; 12; 16; 18; 23; 24; 27; 29; 81; 82; 89; 90; 91	Yes
17	Hardware-Assisted Verification	3; 13; 16; 65	3	RTL Power Consumption Analysis	2; 12; 17; 81; 82	Yes
			13	Debug Verification	6; 7; 12; 14; 15; 17; 52; 61; 64; 66; 67; 68; 82	
			16	Emulation-Based Power Analysis	17	
18	Place & Route	12; 15; 20; 22; 23; 25; 27; 30; 31	7	Static Verification	2; 5; 18	
			12	Simulation Verification	2; 5; 6; 7; 15; 18; 23; 31; 52; 61; 68	
			20	Equivalence Checking	2; 5; 18	
			22	ESD Analysis	18; 27; 35; 45; 60; 73; 89; 90; 91; 92; 93	Yes
			23	Timing Analysis	9; 18; 19; 24; 27; 30; 60; 75; 81; 92; 93; 94; 95; 96; 97	
			25	Clock Jitter Analysis	18; 27; 81; 89; 90; 91; 92; 93	Yes
			27	Parasitic Extraction	18; 21; 35; 39; 56; 60; 69	
			30	Gate-level Power Integrity Analysis	3; 8; 12; 16; 18; 23; 24; 27; 29; 81; 82; 89; 90; 91	Yes
			31	Gate-level Security Analysis	5; 12; 18; 23; 27; 29; 81; 82; 89; 90; 91	Yes
21	Physical Verification	18; 27; 32; 45; 73; 84	18	Place & Route	5; 8; 9; 15; 19; 21; 24; 53; 60; 92; 93; 94; 95; 96; 97	
			27	Parasitic Extraction	18; 21; 35; 39; 56; 60; 69	
			32	Schematic Editing	36; 39	
			84	Mask Tools	21; 39; 69	
23	Timing Analysis	30; 31; 50; 64	12	Simulation Verification	2; 5; 6; 7; 15; 18; 23; 31; 52; 61; 68	
			30	Gate-level Power Integrity Analysis	3; 8; 12; 16; 18; 23; 24; 27; 29; 81; 82; 89; 90; 91	Yes
			31	Gate-level Security Analysis	5; 12; 18; 23; 27; 29; 81; 82; 89; 90; 91	Yes
			33	Circuit Simulation	23; 34; 36; 43; 44; 45; 49; 51; 55; 57; 60; 75; 76; 79; 80; 86	

Exporting functional level IDs	Exporting function (L3)	Full list of Exporting Segment IDs	Importing functional level IDs	Importing function (L3)	Full list of Importing Segment IDs	Affected non-horizontally
24	ECO	18; 23; 30	18	Place & Route	5; 8; 9; 15; 19; 21; 24; 53; 60; 92; 93; 94; 95; 96; 97	
			23	Timing Analysis	9; 18; 19; 24; 27; 30; 60; 75; 81; 92; 93; 94; 95; 96; 97	
			30	Gate-level Power Integrity Analysis	3; 8; 12; 16; 18; 23; 24; 27; 29; 81; 82; 89; 90; 91	Yes
26	Electromagnetic Modelling	50	33	Circuit Simulation	23; 34; 36; 43; 44; 45; 49; 51; 55; 57; 60; 75; 76; 79; 80; 86	Yes
27	Parasitic Extraction	8; 22; 23; 25; 30; 31; 37; 40; 41; 42; 44; 46; 50; 70	8	Gate-level Power Consumption Analysis	2; 3; 5; 12; 16; 27; 82	
			22	ESD Analysis	18; 27; 35; 45; 60; 73; 89; 90; 91; 92; 93	Yes
			23	Timing Analysis	9; 18; 19; 24; 27; 30; 60; 75; 81; 92; 93; 94; 95; 96; 97	
			25	Clock Jitter Analysis	18; 27; 81; 89; 90; 91; 92; 93	Yes
			28	Parasitic Analysis	35; 45; 89; 90; 91	Yes
			30	Gate-level Power Integrity Analysis	3; 8; 12; 16; 18; 23; 24; 27; 29; 81; 82; 89; 90; 91	Yes
			31	Gate-level Security Analysis	5; 12; 18; 23; 27; 29; 81; 82; 89; 90; 91	Yes
			33	Circuit Simulation	23; 34; 36; 43; 44; 45; 49; 51; 55; 57; 60; 75; 76; 79; 80; 86	
			37	Early Power Integrity Analysis	35; 45; 89; 90; 91; 92; 93	Yes
			41	Transistor-level Power Integrity Analysis	33; 35; 45; 51; 53; 60	Yes
			42	Power Device Analysis	33; 35; 45; 89; 90; 91	Yes
			44	Electromagnetic Extraction	35; 45; 89; 90; 91; 92; 93	Yes
29	Design Robustness	30; 31	30	Gate-level Power Integrity Analysis	3; 8; 12; 16; 18; 23; 24; 27; 29; 81; 82; 89; 90; 91	Yes
			31	Gate-level Security Analysis	5; 12; 18; 23; 27; 29; 81; 82; 89; 90; 91	Yes
30	Gate-level Power Integrity Analysis	23; 24; 35	23	Timing Analysis	9; 18; 19; 24; 27; 30; 60; 75; 81; 92; 93; 94; 95; 96; 97	Yes
			24	ECO	30	Yes
			35	Layout	30; 32; 36; 44; 49; 54; 72	Yes
31	Gate-level Security Analysis	12	12	Simulation Verification	2; 5; 6; 7; 15; 18; 23; 31; 52; 61; 68	Yes
32	Schematic Editing	35; 39; 51	21	Physical Verification	32; 56; 60	
			34	Design Environment	32; 33; 41; 47; 50; 52; 55; 57; 60; 77	
			35	Layout	30; 32; 36; 44; 49; 54; 72	
33	Circuit Simulation	34; 41; 42; 51; 79; 80	34	Design Environment	32; 33; 41; 47; 50; 52; 55; 57; 60; 77	
			41	Transistor-level Power Integrity Analysis	33; 35; 45; 51; 53; 60	Yes
			42	Power Device Analysis	33; 35; 45; 89; 90; 91	Yes
			79	PCB Analysis	50	Yes
			80	Packaging	50	Yes

Exporting functional level IDs	Exporting function (L3)	Full list of Exporting Segment IDs	Importing functional level IDs	Importing function (L3)	Full list of Importing Segment IDs	Affected non-horizontally
34	Design Environment	33; 41; 50; 55; 57; 81	33	Circuit Simulation	23; 34; 36; 43; 44; 45; 49; 51; 55; 57; 60; 75; 76; 79; 80; 86	
			41	Transistor-level Power Integrity Analysis	33; 35; 45; 51; 53; 60	Yes
			55	Photonic Chip Simulation	34; 51; 54	
			81	Characterization	51	
35	Layout	36; 37; 40; 41; 42; 43; 44; 45; 46; 49	22	ESD Analysis	18; 27; 35; 45; 60; 73; 89; 90; 91; 92; 93	
			26	Electromagnetic Modelling	35; 89; 90; 91; 92; 93	
			27	Parasitic Extraction	18; 21; 35; 39; 56; 60; 69	
			28	Parasitic Analysis	35; 45; 89; 90; 91	Yes
			36	Electromagnetic Device Synthesis	35; 89; 90; 91; 92; 93	
			37	Early Power Integrity Analysis	35; 45; 89; 90; 91; 92; 93	
			41	Transistor-level Power Integrity Analysis	33; 35; 45; 51; 53; 60	Yes
			42	Power Device Analysis	33; 35; 45; 89; 90; 91	Yes
			44	Electromagnetic Extraction	35; 45; 89; 90; 91; 92; 93	
			49	Electromagnetic Simulation	35; 56	Yes
36	Electromagnetic Device Synthesis	32; 35; 50	32	Schematic Editing	36; 39	
			33	Circuit Simulation	23; 34; 36; 43; 44; 45; 49; 51; 55; 57; 60; 75; 76; 79; 80; 86	Yes
			35	Layout	30; 32; 36; 44; 49; 54; 72	
41	Transistor-level Power Integrity Analysis	35; 51; 60	34	Design Environment	32; 33; 41; 47; 50; 52; 55; 57; 60; 77	Yes
			35	Layout	30; 32; 36; 44; 49; 54; 72	Yes
			60	Architectural Design & Implementation	72; 74; 75	Yes
44	Electromagnetic Extraction	35; 77	33	Circuit Simulation	23; 34; 36; 43; 44; 45; 49; 51; 55; 57; 60; 75; 76; 79; 80; 86	Yes
			35	Layout	30; 32; 36; 44; 49; 54; 72	
47	Reliability Analysis	51; 60	34	Design Environment	32; 33; 41; 47; 50; 52; 55; 57; 60; 77	
			60	Architectural Design & Implementation	72; 74; 75	
49	Electromagnetic Simulation	33; 35	33	Circuit Simulation	23; 34; 36; 43; 44; 45; 49; 51; 55; 57; 60; 75; 76; 79; 80; 86	Yes
			35	Layout	30; 32; 36; 44; 49; 54; 72	Yes
52	Co-Simulation Enabling Kit	12; 13; 34	12	Simulation Verification	2; 5; 6; 7; 15; 18; 23; 31; 52; 61; 68	
			13	Debug Verification	6; 7; 12; 14; 15; 17; 52; 61; 64; 66; 67; 68; 82	
			34	Design Environment	32; 33; 41; 47; 50; 52; 55; 57; 60; 77	

Exporting functional level IDs	Exporting function (L3)	Full list of Exporting Segment IDs	Importing functional level IDs	Importing function (L3)	Full list of Importing Segment IDs	Affected non-horizontally
53	Co-Design Enabling Kit	18; 41	18	Place & Route	5; 8; 9; 15; 19; 21; 24; 53; 60; 92; 93; 94; 95; 96; 97	
			41	Transistor-level Power Integrity Analysis	33; 35; 45; 51; 53; 60	Yes
54	Photonic Layout Design Implementation	35; 39; 45; 49; 55; 56; 57	21	Physical Verification	32; 56; 60	
			27	Parasitic Extraction	18; 21; 35; 39; 56; 60; 69	
			35	Layout	30; 32; 36; 44; 49; 54; 72	
			49	Electromagnetic Simulation	35; 56	Yes
			54	Photonic Layout Design Implementation	54	
			55	Photonic Chip Simulation	34; 51; 54	
55	Photonic Chip Simulation	33; 34; 50; 51	33	Circuit Simulation	23; 34; 36; 43; 44; 45; 49; 51; 55; 57; 60; 75; 76; 79; 80; 86	Yes
			34	Design Environment	32; 33; 41; 47; 50; 52; 55; 57; 60; 77	
60	Architectural Design & Implementation	18; 34; 69; 70; 71; 72; 73; 75; 76; 77	18	Place & Route	5; 8; 9; 15; 19; 21; 24; 53; 60; 92; 93; 94; 95; 96; 97	
			21	Physical Verification	32; 56; 60	
			22	ESD Analysis	18; 27; 35; 45; 60; 73; 89; 90; 91; 92; 93	
			23	Timing Analysis	9; 18; 19; 24; 27; 30; 60; 75; 81; 92; 93; 94; 95; 96; 97	
			27	Parasitic Extraction	18; 21; 35; 39; 56; 60; 69	
			33	Circuit Simulation	23; 34; 36; 43; 44; 45; 49; 51; 55; 57; 60; 75; 76; 79; 80; 86	
			34	Design Environment	32; 33; 41; 47; 50; 52; 55; 57; 60; 77	
			41	Transistor-level Power Integrity Analysis	33; 35; 45; 51; 53; 60	Yes
			75	Structural and Thermal Analysis	60	Yes
			76	Signal and Power Integrity	60	Yes
75	Structural and Thermal Analysis	58; 60; 71	23	Timing Analysis	9; 18; 19; 24; 27; 30; 60; 75; 81; 92; 93; 94; 95; 96; 97	Yes
			33	Circuit Simulation	23; 34; 36; 43; 44; 45; 49; 51; 55; 57; 60; 75; 76; 79; 80; 86	Yes
			60	Architectural Design & Implementation	72; 74; 75	Yes
76	Signal and Power Integrity	77	33	Circuit Simulation	23; 34; 36; 43; 44; 45; 49; 51; 55; 57; 60; 75; 76; 79; 80; 86	Yes
79	PCB Analysis	50	33	Circuit Simulation	23; 34; 36; 43; 44; 45; 49; 51; 55; 57; 60; 75; 76; 79; 80; 86	Yes
80	Packaging	50	33	Circuit Simulation	23; 34; 36; 43; 44; 45; 49; 51; 55; 57; 60; 75; 76; 79; 80; 86	Yes

Exporting functional level IDs	Exporting function (L3)	Full list of Exporting Segment IDs	Importing functional level IDs	Importing function (L3)	Full list of Importing Segment IDs	Affected non-horizontally
81	Characterization	3; 23; 25; 30; 31	3	RTL Power Consumption Analysis	2; 12; 17; 81; 82	Yes
			23	Timing Analysis	9; 18; 19; 24; 27; 30; 60; 75; 81; 92; 93; 94; 95; 96; 97	
			25	Clock Jitter Analysis	18; 27; 81; 89; 90; 91; 92; 93	Yes
			30	Gate-level Power Integrity Analysis	3; 8; 12; 16; 18; 23; 24; 27; 29; 81; 82; 89; 90; 91	Yes
			31	Gate-level Security Analysis	5; 12; 18; 23; 27; 29; 81; 82; 89; 90; 91	Yes
82	Functional Safety & Specification Analysis	3; 8; 13; 30; 31	3	RTL Power Consumption Analysis	2; 12; 17; 81; 82	Yes
			8	Gate-level Power Consumption Analysis	2; 3; 5; 12; 16; 27; 82	Yes
			13	Debug Verification	6; 7; 12; 14; 15; 17; 52; 61; 64; 66; 67; 68; 82	Yes
			30	Gate-level Power Integrity Analysis	3; 8; 12; 16; 18; 23; 24; 27; 29; 81; 82; 89; 90; 91	Yes
			31	Gate-level Security Analysis	5; 12; 18; 23; 27; 29; 81; 82; 89; 90; 91	Yes
86	TCAD	50	33	Circuit Simulation	23; 34; 36; 43; 44; 45; 49; 51; 55; 57; 60; 75; 76; 79; 80; 86	
89	Embedded Memories	22; 25; 30; 31; 36; 37; 42; 43; 44; 46	22	ESD Analysis	18; 27; 35; 45; 60; 73; 89; 90; 91; 92; 93	Yes
			25	Clock Jitter Analysis	18; 27; 81; 89; 90; 91; 92; 93	Yes
			26	Electromagnetic Modelling	35; 89; 90; 91; 92; 93	Yes
			28	Parasitic Analysis	35; 45; 89; 90; 91	Yes
			30	Gate-level Power Integrity Analysis	3; 8; 12; 16; 18; 23; 24; 27; 29; 81; 82; 89; 90; 91	Yes
			31	Gate-level Security Analysis	5; 12; 18; 23; 27; 29; 81; 82; 89; 90; 91	Yes
			36	Electromagnetic Device Synthesis	35; 89; 90; 91; 92; 93	Yes
			37	Early Power Integrity Analysis	35; 45; 89; 90; 91; 92; 93	Yes
			42	Power Device Analysis	33; 35; 45; 89; 90; 91	Yes
			44	Electromagnetic Extraction	35; 45; 89; 90; 91; 92; 93	Yes
90	NVM Other Memory Compilers	22; 25; 30; 31; 36; 37; 42; 43; 44; 46	22	ESD Analysis	18; 27; 35; 45; 60; 73; 89; 90; 91; 92; 93	
			25	Clock Jitter Analysis	18; 27; 81; 89; 90; 91; 92; 93	Yes
			26	Electromagnetic Modelling	35; 89; 90; 91; 92; 93	
			28	Parasitic Analysis	35; 45; 89; 90; 91	Yes
			30	Gate-level Power Integrity Analysis	3; 8; 12; 16; 18; 23; 24; 27; 29; 81; 82; 89; 90; 91	Yes
			31	Gate-level Security Analysis	5; 12; 18; 23; 27; 29; 81; 82; 89; 90; 91	Yes
			36	Electromagnetic Device Synthesis	35; 89; 90; 91; 92; 93	
			37	Early Power Integrity Analysis	35; 45; 89; 90; 91; 92; 93	
			42	Power Device Analysis	33; 35; 45; 89; 90; 91	Yes
			44	Electromagnetic Extraction	35; 45; 89; 90; 91; 92; 93	

Exporting functional level IDs	Exporting function (L3)	Full list of Exporting Segment IDs	Importing functional level IDs	Importing function (L3)	Full list of Importing Segment IDs	Affected non-horizontally
91	Physical Libraries	22; 25; 30; 31; 36; 37; 42; 43; 44; 46	22	ESD Analysis	18; 27; 35; 45; 60; 73; 89; 90; 91; 92; 93	Yes
			25	Clock Jitter Analysis	18; 27; 81; 89; 90; 91; 92; 93	Yes
			26	Electromagnetic Modelling	35; 89; 90; 91; 92; 93	Yes
			28	Parasitic Analysis	35; 45; 89; 90; 91	Yes
			30	Gate-level Power Integrity Analysis	3; 8; 12; 16; 18; 23; 24; 27; 29; 81; 82; 89; 90; 91	Yes
			31	Gate-level Security Analysis	5; 12; 18; 23; 27; 29; 81; 82; 89; 90; 91	Yes
			36	Electromagnetic Device Synthesis	35; 89; 90; 91; 92; 93	Yes
			37	Early Power Integrity Analysis	35; 45; 89; 90; 91; 92; 93	Yes
			42	Power Device Analysis	33; 35; 45; 89; 90; 91	Yes
			44	Electromagnetic Extraction	35; 45; 89; 90; 91; 92; 93	Yes
92	Wired Interface IP	5; 11; 18; 22; 23; 25; 36; 37; 43; 44	5	RTL Synthesis	2; 7; 9; 10; 11; 19; 62; 63; 92; 93; 94; 95; 96; 97	
			11	Design-for-Test / Test IP	92; 93; 94; 95; 96; 97	
			18	Place & Route	5; 8; 9; 15; 19; 21; 24; 53; 60; 92; 93; 94; 95; 96; 97	
			22	ESD Analysis	18; 27; 35; 45; 60; 73; 89; 90; 91; 92; 93	Yes
			23	Timing Analysis	9; 18; 19; 24; 27; 30; 60; 75; 81; 92; 93; 94; 95; 96; 97	
			25	Clock Jitter Analysis	18; 27; 81; 89; 90; 91; 92; 93	Yes
			26	Electromagnetic Modelling	35; 89; 90; 91; 92; 93	Yes
			36	Electromagnetic Device Synthesis	35; 89; 90; 91; 92; 93	Yes
			37	Early Power Integrity Analysis	35; 45; 89; 90; 91; 92; 93	Yes
			44	Electromagnetic Extraction	35; 45; 89; 90; 91; 92; 93	Yes
93	Wireless Interface IP	5; 11; 18; 22; 23; 25; 36; 37; 43; 44	5	RTL Synthesis	2; 7; 9; 10; 11; 19; 62; 63; 92; 93; 94; 95; 96; 97	
			11	Design-for-Test / Test IP	92; 93; 94; 95; 96; 97	
			18	Place & Route	5; 8; 9; 15; 19; 21; 24; 53; 60; 92; 93; 94; 95; 96; 97	
			22	ESD Analysis	18; 27; 35; 45; 60; 73; 89; 90; 91; 92; 93	
			23	Timing Analysis	9; 18; 19; 24; 27; 30; 60; 75; 81; 92; 93; 94; 95; 96; 97	
			25	Clock Jitter Analysis	18; 27; 81; 89; 90; 91; 92; 93	Yes
			26	Electromagnetic Modelling	35; 89; 90; 91; 92; 93	
			36	Electromagnetic Device Synthesis	35; 89; 90; 91; 92; 93	
			37	Early Power Integrity Analysis	35; 45; 89; 90; 91; 92; 93	
			44	Electromagnetic Extraction	35; 45; 89; 90; 91; 92; 93	

Exporting functional level IDs	Exporting function (L3)	Full list of Exporting Segment IDs	Importing functional level IDs	Importing function (L3)	Full list of Importing Segment IDs	Affected non-horizontally
94	Security IP	5; 11; 18; 23	5	RTL Synthesis	2; 7; 9; 10; 11; 19; 62; 63; 92; 93; 94; 95; 96; 97	
			11	Design-for-Test / Test IP	92; 93; 94; 95; 96; 97	
			18	Place & Route	5; 8; 9; 15; 19; 21; 24; 53; 60; 92; 93; 94; 95; 96; 97	
			23	Timing Analysis	9; 18; 19; 24; 27; 30; 60; 75; 81; 92; 93; 94; 95; 96; 97	
95	CPU IP	5; 11; 18; 23	5	RTL Synthesis	2; 7; 9; 10; 11; 19; 62; 63; 92; 93; 94; 95; 96; 97	
			11	Design-for-Test / Test IP	92; 93; 94; 95; 96; 97	
			18	Place & Route	5; 8; 9; 15; 19; 21; 24; 53; 60; 92; 93; 94; 95; 96; 97	
			23	Timing Analysis	9; 18; 19; 24; 27; 30; 60; 75; 81; 92; 93; 94; 95; 96; 97	
96	DSP IP	5; 11; 18; 23	5	RTL Synthesis	2; 7; 9; 10; 11; 19; 62; 63; 92; 93; 94; 95; 96; 97	
			11	Design-for-Test / Test IP	92; 93; 94; 95; 96; 97	
			18	Place & Route	5; 8; 9; 15; 19; 21; 24; 53; 60; 92; 93; 94; 95; 96; 97	
			23	Timing Analysis	9; 18; 19; 24; 27; 30; 60; 75; 81; 92; 93; 94; 95; 96; 97	
97	Other Excl Security IP	5; 11; 18; 23	5	RTL Synthesis	2; 7; 9; 10; 11; 19; 62; 63; 92; 93; 94; 95; 96; 97	
			11	Design-for-Test / Test IP	92; 93; 94; 95; 96; 97	
			18	Place & Route	5; 8; 9; 15; 19; 21; 24; 53; 60; 92; 93; 94; 95; 96; 97	
			23	Timing Analysis	9; 18; 19; 24; 27; 30; 60; 75; 81; 92; 93; 94; 95; 96; 97	

Source: Reply to RFI 19, Annex Q.3.1. M.11481 - Paper on the Lack of Interoperability Concerns - Confidential, November 11, 2024., Annex I.

4.2 EDA functions without interoperability relationships

(52) The interoperability matrix excludes EDA functions that do not fall within a specific design flow (Segment IDs 83 and 85) and legacy tools with non-material revenues (Segment ID 88). In addition, the interoperability matrix excludes functional segments that neither import nor export information from other EDA functional segments:[34]

1) Early Architectural Exploration (Functional ID 4);
2) Electromagnetic modelling (Functional ID 26);
3) Parasitic Analysis (Functional ID 28);
4) Equivalence Checking (Functional ID 38);
5) Thermal Analysis (Functional ID 48);

[34] Reply to RFI 21, para 1.1 and Table 1.

6) Early Architectural Exploration (Functional ID 59);

7) HAT (Functional ID 83);

8) Synthesis (Functional ID 85);

9) Virtual Prototyping (Functional ID 87);

(53) This means that for these EDA functions interoperability cannot be degraded. However, conglomerate effects might still be possible due to bundling strategies, as discussed in the Decision, Section 5.4.

* * *

Case M.11481 – SYNOPSYS/ANSYS

COMMITMENTS TO THE EUROPEAN COMMISSION

Pursuant to Article 6(2) of Council Regulation (EC) No 139/2004 (the "***Merger Regulation***"), Synopsys, Inc. ("***Synopsys***") (the "***Notifying Party***") and Ansys, Inc. ("***Ansys***") hereby enter into the following Commitments (the "***Commitments***") vis-à-vis the European Commission (the "***Commission***") with a view to rendering Synopsys' proposed acquisition of sole control of Ansys (the "***Concentration***") compatible with the internal market and the functioning of the EEA Agreement.

This text shall be interpreted in light of the Commission's decision pursuant to Article 6(1)(b) of the Merger Regulation, to declare the Concentration compatible with the internal market and the functioning of the EEA Agreement (the "***Decision***"), in the general framework of European Union law, in particular in light of the Merger Regulation, and by reference to the Commission Notice on remedies acceptable under Council Regulation (EC) No 139/2004 and under Commission Regulation (EC) No 802/2004 (the "***Remedies Notice***").

The Commitments shall take effect upon the Effective Date, provided that if the completion of the Concentration does not subsequently take place for whatever reason and is thereby abandoned, the Notifying Party and Ansys shall not be bound by these Commitments. These Commitments shall apply to Ansys only in respect of the PCA Divestment Business (as defined in Section A).

Section A. Definitions

1. For the purpose of the Commitments, the following terms shall have the following meaning:

   Ansys: ANSYS, Inc., incorporated under the laws of Delaware, U.S., with its registered office at 2600 ANSYS Drive, Canonsburg, PA, 15317, United States and registered with EIN number 04-3219960.

   Affiliated Undertakings: undertakings controlled by the Parties and/or by the ultimate parents of the Parties, whereby the notion of control shall be interpreted pursuant to Article 3 of the Merger Regulation and in light of the Commission Consolidated Jurisdictional Notice under Council Regulation (EC) No 139/2004 on the control of concentrations between undertakings (the "***Consolidated Jurisdictional Notice***").

   Assets: the assets that contribute to the current operation or are necessary to ensure the viability and competitiveness of the Divestment Business as indicated in Section B, paragraph (a), (b) and (c) and described more in detail in the Schedules.

   Closing: the transfer of the legal title to the Divestment Business to the Purchaser(s).

   Closing Period: the longer of the period of […] from the approval of the Purchaser(s) and the terms of sale by the Commission, or the period until […] after completion of Synopsys' acquisition of Ansys.

   Confidential Information: any business secrets, know-how, commercial information, or any other information of a proprietary nature that is not in the public domain.

Conflict of Interest: any conflict of interest that impairs the Trustee's objectivity and independence in discharging its duties under the Commitments.

Divestment Business: the OSG Divestment Business and the PCA Divestment Business.

Divestiture Trustee: one or more natural or legal person(s) who is/are approved by the Commission and appointed by the Notifying Party and Ansys and who has/have received from the Notifying Party and Ansys the exclusive Trustee Mandate to sell the Divestment Business to a Purchaser at no minimum price.

Effective Date: the date of adoption of the Decision.

First Divestiture Period: the period of […] from the Effective Date.

Hold Separate Manager: the person(s) appointed by the Notifying Party and Ansys for the Divestment Business to manage the day-to-day business under the supervision of the Monitoring Trustee.

Key Personnel: all personnel necessary to maintain the viability and competitiveness of the Divestment Business, as listed in the Schedules, including the Hold Separate Manager.

Monitoring Trustee: one or more natural or legal person(s) who is/are approved by the Commission and appointed by the Notifying Party and Ansys, and who has/have the duty to monitor the Notifying Party and Ansys's compliance with the conditions and obligations attached to the Decision.

OSG Divestment Business: Synopsys' entire optical and photonics device simulation business, the Optical Solutions Group ("OSG"), as defined in Section B and in the Schedules, which the Notifying Party commits to divest.

Parties: the Notifying Party and Ansys.

Personnel: all staff currently employed by the Divestment Business, including staff seconded to the Divestment Business, shared personnel as listed in the Schedules.

PCA Divestment Business: the business comprised of researching, developing, distributing, licensing, selling, marketing, commercializing and otherwise making available the register-transfer-level ("RTL") Power Consumption Analysis ("PCA") product commercially distributed by Ansys as *PowerArtist*, as defined in Section B and in the Schedules, which the Notifying Party and Ansys commit to divest.

Purchaser(s): the entity(ies) approved by the Commission as acquirer(s) of the OSG Divestment Business and the PCA Divestment Business in accordance with the criteria set out in Section D.

Purchaser Criteria: the criteria laid down in paragraph 18 of these Commitments that the Purchaser must fulfil in order to be approved by the Commission.

Schedules: the schedules to these Commitments describing more in detail the OSG Divestment Business and the PCA Divestment Business.

Synopsys: Synopsys, Inc., incorporated under the laws of Delaware, U.S., with its registered office at 675 Almanor Avenue, Sunnyvale, CA, 94085, United States and registered with EIN number 56-1546236.

Trustee(s): the Monitoring Trustee and/or the Divestiture Trustee as the case may be.

Trustee Divestiture Period: the period of […] from the end of the First Divestiture Period.

Section B. The commitment to divest and the Divestment Business

Commitment to divest

2. In order to maintain effective competition, the Notifying Party and Ansys commit to divest, or procure the divestiture of the OSG Divestment Business and of the PCA Divestment Business by the end of the Trustee Divestiture Period as a going concern to a purchaser(s) and on terms of sale approved by the Commission in accordance with the procedure described in paragraph 19 of these Commitments. To carry out the divestiture, the Notifying Party and Ansys commit to find a purchaser(s) and to enter into a final binding sale and purchase agreement for the sale of the Divestment Business within the First Divestiture Period. If the Notifying Party and Ansys have not entered into such an agreement at the end of the First Divestiture Period, the Notifying Party and Ansys shall grant the Divestiture Trustee an exclusive mandate to sell the Divestment Business in accordance with the procedure described in paragraph 31 in the Trustee Divestiture Period.

3. The proposed concentration shall not be implemented before the Notifying Party, Ansys or the Divestiture Trustee has entered into a final binding sale and purchase agreement for the sale of the Divestment Business and the Commission has approved the Purchaser and the terms of sale in accordance with Paragraph 19.

4. The Notifying Party and Ansys shall be deemed to have complied with this commitment if:

   (a) by the end of the Trustee Divestiture Period, the Notifying Party and Ansys or the Divestiture Trustee have entered into a final binding sale and purchase agreement and the Commission approves the proposed purchaser(s) and the terms of sale as being consistent with the Commitments in accordance with the procedure described in paragraph 19; and

   (b) the Closing of the sale of the Divestment Business to the Purchaser(s) takes place within the Closing Period.

5. In order to maintain the structural effect of the Commitments, the Notifying Party and Ansys shall, for a period of […] after Closing, not acquire, whether directly or indirectly, the possibility of exercising influence (as defined in paragraph 43 of the Remedies Notice, footnote 3) over the whole or part of the Divestment Business, unless, following the submission of a reasoned request from the Notifying Party or Ansys showing good cause and accompanied by a report from the Monitoring Trustee (as provided in paragraph 45 of these Commitments), the Commission finds that the structure of the market has changed to such an extent that the absence of influence over the Divestment

Business is no longer necessary to render the proposed concentration compatible with the internal market.

Structure and definition of the Divestment Business

6. The OSG Divestment Business consists of Synopsys' entire optical and photonics device simulation business, the Optical Solutions Group. The legal and functional structure of the OSG Divestment Business as operated to date is described in Schedule I. The OSG Divestment Business, described in more detail in Schedule I, includes all assets that contribute to the current operation or are necessary to ensure the viability and competitiveness of the Divestment Business, in particular:

   (a) all tangible and intangible assets (including intellectual property rights);

   (b) all licenses, permits and authorizations issued by any governmental organization for the benefit of the Divestment Business;

   (c) all contracts,[1] leases, commitments and customer orders of the Divestment Business; all customer, credit and other records of the Divestment Business; and

   (d) the Personnel.

7. In addition, the OSG Divestment Business includes the benefit, for transitional periods, as detailed in Schedule I, on terms and conditions equivalent to those at present afforded to the OSG Divestment Business, of all current arrangements under which Synopsys or its Affiliated Undertakings supply products or services to the OSG Divestment Business, as detailed in Schedule I, unless otherwise agreed with the Purchaser. Strict firewall procedures will be adopted so as to ensure that any competitively sensitive information related to, or arising from such supply arrangements (for example, product roadmaps) will not be shared with, or passed on to, anyone other than for the purpose of the implementation of the Commitments.

8. The PCA Divestment Business consists of Ansys' register-transfer level ("RTL") Power Consumption Analysis tool and related assets as detailed in Schedule II. The legal and functional structure of the PCA Divestment Business as operated to date is described in Schedule II. The PCA Divestment Business, described in more detail in the Schedule, includes all assets and staff that contribute to the current operation or are necessary to ensure the viability and competitiveness of the PCA Divestment Business, in particular:

   (a) all intangible assets (including intellectual property rights);

   (b) all licences, permits and authorisations issued by any governmental organisation for the benefit of the PCA Divestment Business;

   (c) all contracts, leases, commitments and customer orders of the Divestment Business; all customer, credit and other records of the PCA Divestment Business; and

[1] See paragraph 2 of Schedule I below.

(d) the Personnel.

9. In addition, the PCA Divestment Business includes the benefit, for transitional periods, as detailed in Schedule II, on terms and conditions equivalent to those at present afforded to the Divestment Business, of all current arrangements under which Ansys or its Affiliated Undertakings supply products or services to the Divestment Business, as detailed in Schedule II, unless otherwise agreed with the Purchaser. Strict firewall procedures will be adopted so as to ensure that any competitively sensitive information related to, or arising from such supply arrangements (for example, product roadmaps) will not be shared with, or passed on to, anyone other than for the purpose of the implementation of the Commitments.

Section C. Related commitments

Preservation of viability, marketability and competitiveness

10. From the Effective Date until Closing, the Notifying Party and Ansys shall preserve or procure the preservation of the economic viability, marketability and competitiveness of the Divestment Business, in accordance with good business practice, and shall minimise as far as possible any risk of loss of competitive potential of the Divestment Business. In particular the Notifying Party and Ansys undertake:

(a) not to carry out any action that might have a significant adverse impact on the value, management or competitiveness of the Divestment Business or that might alter the nature and scope of activity, or the industrial or commercial strategy or the investment policy of the Divestment Business;

(b) to make available, or procure to make available, sufficient resources for the development of the Divestment Business, on the basis and continuation of the existing business plans;

(c) to take all reasonable steps, or procure that all reasonable steps are being taken, including appropriate incentive schemes (based on industry practice), to encourage all Key Personnel to remain with the Divestment Business, and not to solicit or move any Personnel to the Notifying Party's or Ansys' remaining business. Where, nevertheless, individual members of the Key Personnel exceptionally leave the Divestment Business, the Notifying Party or Ansys shall provide a reasoned proposal to replace the person or persons concerned to the Commission and the Monitoring Trustee. The Notifying Party or Ansys must be able to demonstrate to the Commission that the replacement is well suited to carry out the functions exercised by those individual members of the Key Personnel. The replacement shall take place under the supervision of the Monitoring Trustee, who shall report to the Commission.

Hold-separate obligations

11. The Notifying Party and Ansys commit, from the Effective Date until Closing, to procure that the Divestment Business is kept separate from the business(es) that the Notifying Party and Ansys will be retaining and, after closing of the notified transaction, to keep the Divestment Business Separate from the business that the Notifying Party and Ansys are retaining, and to ensure that unless explicitly permitted under these

Commitments: (i) management and staff of the business(es) retained by the Notifying Party or Ansys have no involvement in the Divestment Business; (ii) the Key Personnel and Personnel of the Divestment Business have no involvement in any business retained by the Notifying Party or Ansys and do not report to any individual outside the Divestment Business.

12. Until Closing, the Notifying Party and Ansys shall assist the Monitoring Trustee in ensuring that the Divestment Business is managed as a distinct and saleable entity separate from the business(es) which the Notifying Party or Ansys is retaining. Immediately after the adoption of the Decision, the Notifying Party and Ansys shall appoint a Hold Separate Manager. The Hold Separate Manager, who shall be part of the Key Personnel, shall manage the Divestment Business independently and in the best interest of the business with a view to ensuring its continued economic viability, marketability and competitiveness and its independence from the businesses retained by the Notifying Party or Ansys. The Hold Separate Manager shall closely cooperate with and report to the Monitoring Trustee and, if applicable, the Divestiture Trustee. Any replacement of the Hold Separate Manager shall be subject to the procedure laid down in paragraph 11(c) of these Commitments. The Commission may, after having heard the Notifying Party or Ansys, require the Notifying Party or Ansys to replace the Hold Separate Manager.

Ring-fencing

13. The Notifying Party and Ansys shall implement, or procure to implement, all necessary measures to ensure that it does not, after the Effective Date, obtain any Confidential Information relating to the Divestment Business and that any such Confidential Information obtained by the Notifying Party or Ansys before the Effective Date will be eliminated and not be used by the Notifying Party or Ansys. This includes measures vis-à-vis the Notifying Party's or Ansys' appointees on the supervisory board and/or board of directors of the Divestment Business. In particular, the participation of the Divestment Business in any central information technology network shall be severed to the extent possible, without compromising the viability of the Divestment Business. The Notifying Party or Ansys may obtain or keep information relating to the Divestment Business which is reasonably necessary for the divestiture of the Divestment Business or the disclosure of which to the Notifying Party or Ansys is required by law.

Non-solicitation clause

14. The Parties undertake, subject to customary limitations, not to solicit, and to procure that Affiliated Undertakings do not solicit, the Key Personnel transferred with the Divestment Business for a period of […] after Closing.

Due diligence

15. In order to enable potential purchasers to carry out a reasonable due diligence of the Divestment Business, the Notifying Party and Ansys shall, subject to customary confidentiality assurances and dependent on the stage of the divestiture process:

    (a) provide to potential purchasers sufficient information as regards the Divestment Business;

(b) provide to potential purchasers sufficient information relating to the Personnel and allow them reasonable access to the Personnel.

Reporting

16. The Notifying Party and Ansys shall submit written reports in English on potential purchasers of the Divestment Business and developments in the negotiations with such potential purchasers to the Commission and the Monitoring Trustee no later than 10 days after the end of every month following the Effective Date (or otherwise at the Commission's request). The Notifying Party and Ansys shall submit a list of all potential purchasers having expressed interest in acquiring the Divestment Business to the Commission at each and every stage of the divestiture process, as well as a copy of all the offers made by potential purchasers within five days of their receipt.

17. The Notifying Party and Ansys shall inform the Commission and the Monitoring Trustee on the preparation of the data room documentation and the due diligence procedure and shall submit a copy of any information memorandum to the Commission and the Monitoring Trustee before sending the memorandum out to potential purchasers.

Section D. The Purchaser

18. In order to be approved by the Commission, the Purchaser must fulfil the following criteria:

(a) The Purchaser shall be independent of and unconnected to the Notifying Party and Ansys and its Affiliated Undertakings (this being assessed having regard to the situation following the divestiture).

(b) The Purchaser shall have the financial resources, proven expertise and incentive to maintain and develop the Divestment Business as a viable and active competitive force in competition with the Parties and other competitors;

(c) The acquisition of the Divestment Business by the Purchaser must neither be likely to create, in light of the information available to the Commission, *prima facie* competition concerns nor give rise to a risk that the implementation of the Commitments will be delayed. In particular, the Purchaser must reasonably be expected to obtain all necessary approvals from the relevant regulatory authorities for the acquisition of the Divestment Business.

(d) The Purchaser of the PCA Divestment Business shall be active in the EDA sector.

19. The final binding sale and purchase agreement (as well as ancillary agreements) relating to the divestment of the Divestment Business shall be conditional on the Commission's approval. When the Notifying Party or Ansys has reached an agreement with a purchaser, it shall submit a fully documented and reasoned proposal, including a copy of the final agreement(s), within one week to the Commission and the Monitoring Trustee. The Notifying Party and Ansys must be able to demonstrate to the Commission that the purchaser fulfils the Purchaser Criteria and that the Divestment Business is being sold in a manner consistent with the Commission's Decision and the Commitments. For the approval, the Commission shall verify that the purchaser fulfils

the Purchaser Criteria and that the Divestment Business is being sold in a manner consistent with the Commitments including their objective to bring about a lasting structural change in the market. The Commission may approve the sale of the Divestment Business without one or more Assets or parts of the Personnel, or by substituting one or more Assets or parts of the Personnel with one or more different assets or different personnel, if this does not affect the viability and competitiveness of the Divestment Business after the sale, taking account of the proposed purchaser.

Section E. Trustee

I. Appointment procedure

20. The Notifying Party and Ansys shall appoint a Monitoring Trustee to carry out the functions specified in these Commitments for a Monitoring Trustee. The Notifying Party and Ansys commit not to close the Concentration before the appointment of a Monitoring Trustee.

21. If the Notifying Party and Ansys have not entered into a binding sale and purchase agreement regarding the Divestment Business one month before the end of the First Divestiture Period, or if the Commission has rejected a purchaser proposed by the Notifying Party and Ansys at that time or thereafter, the Notifying Party and Ansys shall appoint a Divestiture Trustee. The appointment of the Divestiture Trustee shall take effect upon the commencement of the Trustee Divestiture Period.

22. The Trustee shall:

    (a) at the time of appointment, be independent of the Notifying Party and Ansys and their Affiliated Undertakings;

    (b) possess the necessary qualifications to carry out its mandate, for example have sufficient relevant experience as an investment banker or consultant or auditor, as well as relevant experience related to the transfer of intellectual property rights; and

    (c) neither have nor become exposed to a Conflict of Interest.

23. The Trustee shall be remunerated by the Notifying Party and/or Ansys in a way that does not impede the independent and effective fulfilment of its mandate. In particular, where the remuneration package of a Divestiture Trustee includes a success premium linked to the final sale value of the Divestment Business, such success premium may only be earned if the divestiture takes place within the Trustee Divestiture Period.

Proposal by the Notifying Party and Ansys

24. No later than two weeks after the Effective Date, the Notifying Party and Ansys shall submit the name or names of one or more natural or legal persons whom the Notifying Party and Ansys proposes to appoint as the Monitoring Trustee to the Commission for approval. No later than one month before the end of the First Divestiture Period or on request by the Commission, the Notifying Party and shall submit a list of one or more persons whom the Notifying Party proposes to appoint as Divestiture Trustee to the Commission for approval. The proposal shall contain sufficient information for the

Commission to verify that the person or persons proposed as Trustee fulfil the requirements set out in paragraph 22 and shall include:

(a) the full terms of the proposed mandate, which shall include all provisions necessary to enable the Trustee to fulfil its duties under these Commitments;

(b) the outline of a work plan which describes how the Trustee intends to carry out its assigned tasks;

(c) an indication whether the proposed Trustee is to act as both Monitoring Trustee and Divestiture Trustee or whether different trustees are proposed for the two functions.

Approval or rejection by the Commission

25. The Commission shall have the discretion to approve or reject the proposed Trustee(s) and to approve the proposed mandate subject to any modifications it deems necessary for the Trustee to fulfil its obligations. If only one name is approved, the Notifying Party and Ansys shall appoint or cause to be appointed the person or persons concerned as Trustee, in accordance with the mandate approved by the Commission. If more than one name is approved, the Notifying Party and Ansys shall be free to choose the Trustee to be appointed from among the names approved. The Trustee shall be appointed within one week of the Commission's approval, in accordance with the mandate approved by the Commission.

New proposal by the Notifying Party and Ansys

26. If all the proposed Trustees are rejected, the Notifying Party and Ansys shall submit the names of at least two more natural or legal persons within one week of being informed of the rejection, in accordance with paragraphs 20 and 25 of these Commitments.

Trustee nominated by the Commission

27. If all further proposed Trustees are rejected by the Commission, the Commission shall nominate a Trustee, whom the Notifying Party and Ansys shall appoint, or cause to be appointed, in accordance with a trustee mandate approved by the Commission.

II. Functions of the Trustee

28. The Trustee shall assume its specified duties and obligations in order to ensure compliance with the Commitments. The Commission may, on its own initiative or at the request of the Trustee or the Notifying Party and/or Ansys, give any orders or instructions to the Trustee in order to ensure compliance with the conditions and obligations attached to the Decision.

Duties and obligations of the Monitoring Trustee

29. The Monitoring Trustee shall:

(a) propose in its first report to the Commission a detailed work plan describing how it intends to monitor compliance with the obligations and conditions attached to the Decision.

(b) oversee, in close co-operation with the Hold Separate Manager, the on-going management of the Divestment Business with a view to ensuring its continued economic viability, marketability and competitiveness and monitor compliance by the Notifying Party and Ansys with the conditions and obligations attached to the Decision. To that end the Monitoring Trustee shall:

(i) monitor the preservation of the economic viability, marketability and competitiveness of the Divestment Business, and the keeping separate of the Divestment Business from the business retained by the Parties, in accordance with paragraphs 10 and 11 of these Commitments;

(ii) supervise the management of the Divestment Business as a distinct and saleable entity, in accordance with paragraph 12 of these Commitments;

(iii) with respect to Confidential Information:

- determine all necessary measures to ensure that the Notifying Party and Ansys does not after the Effective Date obtain any Confidential Information relating to the Divestment Business,

- in particular strive for the severing of the Divestment Business' participation in a central information technology network to the extent possible, without compromising the viability of the Divestment Business,

- make sure that any Confidential Information relating to the Divestment Business obtained by the Notifying Party or Ansys before the Effective Date is eliminated and will not be used by the Notifying Party or Ansys and

- decide whether such information may be disclosed to or kept by the Notifying Party or Ansys as the disclosure is reasonably necessary to allow the Notifying Party or Ansys to carry out the divestiture or as the disclosure is required by law;

(iv) monitor the splitting of assets and the allocation of Personnel between the Divestment Business and the Notifying Party and/or Ansys or Affiliated Undertakings;

(c) propose to the Notifying Party and/or Ansys such measures as the Monitoring Trustee considers necessary to ensure the Notifying Party's and/or Ansys' compliance with the conditions and obligations attached to the Decision, in particular the maintenance of the full economic viability, marketability or competitiveness of the Divestment Business, the holding separate of the Divestment Business and the non-disclosure of competitively sensitive information;

(d) review and assess potential purchasers as well as the progress of the divestiture process and verify that, dependent on the stage of the divestiture process:

(i) potential purchasers receive sufficient and correct information relating to the Divestment Business and the Personnel in particular by reviewing,

if available, the data room documentation, the information memorandum and the due diligence process, and

(ii) potential purchasers are granted reasonable access to the Personnel;

(e) act as a contact point for any requests by third parties, in particular potential purchasers, in relation to the Commitments;

(f) provide to the Commission, sending the Notifying Party and/or Ansys a non-confidential copy at the same time, a written report within 15 days after the end of every month that shall cover the operation and management of the Divestment Business as well as the splitting of assets and the allocation of Personnel so that the Commission can assess whether the business is held in a manner consistent with the Commitments and the progress of the divestiture process as well as potential purchasers;

(g) promptly report in writing to the Commission, sending the Notifying Party and/or Ansys a non-confidential copy at the same time, if it concludes on reasonable grounds that the Notifying Party and/or Ansys is failing to comply with these Commitments;

(h) within one week after receipt of the documented proposal referred to in paragraph 24 of these Commitments, submit to the Commission, sending the Notifying Party and/or Ansys a non-confidential copy at the same time, a reasoned opinion as to the suitability and independence of the proposed purchaser and the viability of the Divestment Business after the Sale and as to whether the Divestment Business is sold in a manner consistent with the conditions and obligations attached to the Decision, in particular, if relevant, whether the Sale of the Divestment Business without one or more Assets or not all of the Personnel affects the viability of the Divestment Business after the sale, taking account of the proposed purchaser;

(i) assume the other functions assigned to the Monitoring Trustee under the conditions and obligations attached to the Decision.

30. If the Monitoring and Divestiture Trustee are not the same legal or natural persons, the Monitoring Trustee and the Divestiture Trustee shall cooperate closely with each other during and for the purpose of the preparation of the Trustee Divestiture Period in order to facilitate each other's tasks.

Duties and obligations of the Divestiture Trustee

31. Within the Trustee Divestiture Period, the Divestiture Trustee shall sell at no minimum price the Divestment Business to a purchaser, provided that the Commission has approved both the purchaser and the final binding sale and purchase agreement (and ancillary agreements) as in line with the Commission's Decision and the Commitments in accordance with paragraphs 19 and 20 of these Commitments. The Divestiture Trustee shall include in the sale and purchase agreement (as well as in any ancillary agreements) such terms and conditions as it considers appropriate for an expedient sale in the Trustee Divestiture Period. In particular, the Divestiture Trustee may include in the sale and purchase agreement such customary representations and warranties and

indemnities as are reasonably required to effect the sale. The Divestiture Trustee shall protect the legitimate financial interests of the Notifying Party and Ansys, subject to the Notifying Party's and Ansys' unconditional obligation to divest at no minimum price in the Trustee Divestiture Period.

32. In the Trustee Divestiture Period (or otherwise at the Commission's request), the Divestiture Trustee shall provide the Commission with a comprehensive monthly report written in English on the progress of the divestiture process. Such reports shall be submitted within 15 days after the end of every month with a simultaneous copy to the Monitoring Trustee and a non-confidential copy to the Notifying Party and Ansys.

III. Duties and obligations of the Notifying Party and Ansys

33. The Notifying Party and Ansys shall provide and shall cause its advisors to provide the Trustee with all such co-operation, assistance and information as the Trustee may reasonably require to perform its tasks. The Trustee shall have full and complete access to any of the Notifying Party's and Ansys' or the Divestment Business' books, records, documents, management or other personnel, facilities, sites and technical information necessary for fulfilling its duties under the Commitments and the Notifying Party and Ansys and the Divestment Business shall provide the Trustee upon request with copies of any document. The Notifying Party and Ansys and the Divestment Business shall make available to the Trustee one or more offices on their premises and shall be available for meetings in order to provide the Trustee with all information necessary for the performance of its tasks.

34. The Notifying Party and Ansys shall provide the Monitoring Trustee with all managerial and administrative support that it may reasonably request on behalf of the management of the Divestment Business. This shall include all administrative support functions relating to the Divestment Business which are currently carried out at headquarters level. The Notifying Party and Ansys shall provide and shall cause its advisors to provide the Monitoring Trustee, on request, with the information submitted to potential purchasers, in particular give the Monitoring Trustee access to the data room documentation and all other information granted to potential purchasers in the due diligence procedure. The Notifying Party and Ansys shall inform the Monitoring Trustee on possible purchasers, submit lists of potential purchasers at each stage of the selection process, including the offers made by potential purchasers at those stages, and keep the Monitoring Trustee informed of all developments in the divestiture process.

35. The Notifying Party and Ansys shall grant or procure Affiliated Undertakings to grant comprehensive powers of attorney, duly executed, to the Divestiture Trustee to effect the sale (including ancillary agreements), the Closing and all actions and declarations which the Divestiture Trustee considers necessary or appropriate to achieve the sale and the Closing, including the appointment of advisors to assist with the sale process. Upon request of the Divestiture Trustee, the Notifying Party and Ansys shall cause the documents required for effecting the sale and the Closing to be duly executed.

36. The Notifying Party and Ansys shall indemnify the Trustee and its employees and agents (each an "***Indemnified Party***") and hold each Indemnified Party harmless against, and hereby agrees that an Indemnified Party shall have no liability to the Notifying Party and Ansys for, any liabilities arising out of the performance of the Trustee's duties under the Commitments, except to the extent that such liabilities result

from the willful default, recklessness, gross negligence or bad faith of the Trustee, its employees, agents or advisors.

37. At the expense of the Notifying Party and Ansys, the Trustee may appoint advisors (in particular for corporate finance or legal advice), subject to the Notifying Party's and Ansys' approval (this approval not to be unreasonably withheld or delayed) if the Trustee considers the appointment of such advisors necessary or appropriate for the performance of its duties and obligations under the Mandate, provided that any fees and other expenses incurred by the Trustee are reasonable. Should the Notifying Party and Ansys refuse to approve the advisors proposed by the Trustee the Commission may approve the appointment of such advisors instead, after having heard the Notifying Party and Ansys. Only the Trustee shall be entitled to issue instructions to the advisors. Paragraph 36 of these Commitments shall apply *mutatis mutandis*. In the Trustee Divestiture Period, the Divestiture Trustee may use advisors who served the Notifying Party and Ansys during the Divestiture Period if the Divestiture Trustee considers this in the best interest of an expedient sale.

38. The Notifying Party and Ansys agrees that the Commission may share Confidential Information proprietary to the Notifying Party or Ansys with the Trustee. The Trustee shall not disclose such information and the principles contained in Article 17 (1) and (2) of the Merger Regulation apply *mutatis mutandis*.

39. The Notifying Party and Ansys agrees that the contact details of the Monitoring Trustee are published on the website of the Commission's Directorate-General for Competition and they shall inform interested third parties, in particular any potential purchasers, of the identity and the tasks of the Monitoring Trustee.

40. For a period of […] from the Effective Date the Commission may request all information from the Parties that is reasonably necessary to monitor the effective implementation of these Commitments.

IV. Replacement, discharge and reappointment of the Trustee

41. If the Trustee ceases to perform its functions under the Commitments or for any other good cause, including the exposure of the Trustee to a Conflict of Interest:

    (a) the Commission may, after hearing the Trustee and the Notifying Party an Ansys, require the Notifying Party and Ansys to replace the Trustee; or

    (b) the Notifying Party and Ansys may, with the prior approval of the Commission, replace the Trustee.

42. If the Trustee is removed according to paragraph 41 of these Commitments, the Trustee may be required to continue in its function until a new Trustee is in place to whom the Trustee has effected a full hand over of all relevant information. The new Trustee shall be appointed in accordance with the procedure referred to in paragraphs 20-27 of these Commitments.

43. Unless removed according to paragraph 41 of these Commitments, the Trustee shall cease to act as Trustee only after the Commission has discharged it from its duties after all the Commitments with which the Trustee has been entrusted have been implemented. However, the Commission may at any time require the reappointment of the Monitoring

Trustee if it subsequently appears that the relevant remedies might not have been fully and properly implemented.

Section F. The review clause

44. The Commission may extend the time periods foreseen in the Commitments in response to a request from the Notifying Party and/or Ansys or, in appropriate cases, on its own initiative. Where the Notifying Party and/or Ansys requests an extension of a time period, it shall submit a reasoned request to the Commission no later than one month before the expiry of that period, showing good cause**.** This request shall be accompanied by a report from the Monitoring Trustee, who shall, at the same time send a non-confidential copy of the report to the Notifying Party and/or Ansys. Only in exceptional circumstances shall the Notifying Party and/or Ansys be entitled to request an extension within the last month of any period.

45. The Commission may further, in response to a reasoned request from the Notifying Party and/or Ansys, showing good cause waive, modify or substitute, in exceptional circumstances, one or more of the undertakings in these Commitments. This request shall be accompanied by a report from the Monitoring Trustee, who shall, at the same time send a non-confidential copy of the report to the Notifying Party and/or Ansys. The request shall not have the effect of suspending the application of the undertaking and, in particular, of suspending the expiry of any time period in which the undertaking has to be complied with.

Section G. Entry into force

46. The Commitments shall take effect upon the date of adoption of the Decision.

[signed]

[Information on Synopsys' legal representative]
duly authorised for and on behalf of
Synopsys, Inc.

[signed]

[Information on Ansys' legal representative]
duly authorised for and on behalf of
Ansys, Inc.

SCHEDULE I – OSG DIVESTMENT BUSINESS

1. The Divestment Business as operated to date has the following legal and functional structure:

1.1 **General.** The OSG Divestment Business comprises Synopsys' entire optical and photonics device simulation business, the Optical Solutions Group ("OSG").[2] The OSG Divestment Business is a standalone and easily severable business that already operates largely independently from the rest of Synopsys, with [OSG Divestment Business' internal organization within Synopsys.] [3]

1.2 **Legal structure.** The legal entity to be divested will be [name of legal entity]. [information on divestment legal structure].

1.3 **Functional Structure.** The OSG Divestment Business is managed by […] who reports directly to […], head of the [internal organization within Synopsys]. A high-level organization chart is provided at **Figure 1** below.[4]

[2] Synopsys' Photonic Solutions business concerns the design and simulation of photonic chips which use light instead of electrons to transport information. [Photonics Solutions business's internal organization within Synopsys].

[3] See paragraph 3.1 below.

[4] [Description of Synopsys' internal organization].

Figure 1: OSG Divestment Business Organizational Chart[5]

[…]

Source: Synopsys

1.4 In addition, **Figure 2** shows Synopsys' wider organization [Synopsys' internal structure and organization].[6] [OSG Divestment Business' and Synopsys' internal structure and organization].

Figure 2: Organigram of Synopsys' wider organization as of June 2024

[…]

Source: Synopsys

Figure 3: OSG reporting lines towards Synopsys' wider organization as of June 2024

[…]

Source: Synopsys

2. In accordance with paragraph 6 of these Commitments, the Divestment Business includes, but is not limited to:

(a) the following main tangible assets:

2.1 **Offices.** The OSG Divestment Business will include […] facilities: [information on the facilities included in the OSG Divestment Business] dedicated to the OSG Divestment Business. [information on the facilities included in the OSG Divestment Business] R&D lab space [information on the facilities included in the OSG Divestment Business] an office space.

2.2 **Other assets.** This is provided as **Schedule I – Annex I**, and includes assets such as [information on other assets included in the OSG Divestment Business].

[5] [OSG Divestment Business's internal organization within Synopsys].

[6] [Description of Synopsys' internal organization].

(b) the following main intangible assets:

2.3 **Patents.** Synopsys commits that all patents exclusively or predominantly used by the OSG Divestment Business will be transferred. A list of patents pertaining exclusively to the OSG Divestment Business are set out in **Schedule I – Annex II.**

2.4 **Brand Names.** Synopsys will also divest all brand names of the OSG Divestment Business products.

2.5 **All other intellectual property.** Any other intellectual property exclusively or predominantly used by the OSG Divestment Business will also be divested. This includes (*inter alia*) domain names, and all copyrights and trade secrets embodied in the OSG Divestment Business products.

2.6 In addition, Synopsys and the Purchaser will enter into a customary arrangement whereby (i) Synopsys will agree not to enforce its retained IP rights (as they exist as of the time of Closing) against the Purchaser in order to prevent it from operating the OSG Divestment Business, and (ii) the Purchaser will agree not to enforce IP rights transferred with the OSG Divestment Business (as they exist as of the time of Closing) against Synopsys, to the extent any such rights are used in or necessary for the operation of the retained business' activities unrelated to the activities of the OSG Divestment Business. Any such customary arrangement will be set out in the final binding sale and purchase agreement and will be subject to the assessment by the Monitoring Trustee and the Commission's prior approval.

2.7 **Sales.** The OSG Divestment Business will include all sales resources and operations, [information on sales channels of the OSG Divestment Business].[7]

(c) the following main licences, permits and authorisations:

2.8 **Licenses.** Synopsys will provide the Purchaser with the [License 1] and [License 2] system license for a transitional period of at least [duration of the transitional period] and up to [duration of the transitional period] after Closing.

(d) the following main contracts, agreements, leases, commitments and understandings:

2.9 **Customer contracts.** All customer contracts[8] are included in the OSG Divestment Business and will be transferred in their entirety to the Purchaser.

2.10 **Interoperability Agreements.** All interoperability agreements that apply to the tools of the OSG Divestment Business will be divested and transferred with the OSG Divestment Business.

(e) the following customer, credit and other records:

2.11 **Customer records.** The OSG Divestment Business will include all customer records.

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[7] [Information on the OSG Divestment Business's customer contracts].

[8] See paragraph 3.1 below.

(f) the following personnel:

2.12 The OSG Divestment Business will include all employees currently working, full time or part time, on optics and photonics device simulation business activities, including the employees detailed at **Figure 1** above. A detailed breakdown of the current FTE is provided in **Table 1** below.

Table 1: OSG Divestment Business FTEs by department

[…]

Source: Synopsys

(g) the following Key Personnel:

2.13 The following Key Personnel*:* [identity and roles of Key Personnel included in the OSG Divestment Business]

2.14 These individuals are flagged as Key Personnel as they are the most senior individuals involved in the OSG Divestment Business. Respectively, [identity and role of Key Personnel], while [identity and role of Key Personnel], [identity and role of Key Personnel] and [identity and role of Key Personnel] are [functions of Key Personnel]. [9] Additionally, Synopsys has previously identified [identity and role of Key Personnel], [identity and role of Key Personnel], and [identity and role of Key Personnel] as [Synopsys' business strategy].

(h) the arrangements for the supply with the following products or services by Synopsys or Affiliated Undertakings for a transitional period of up to one year after Closing:

2.15 Synopsys commits to enter into TSAs related to IT, facilities, misdirected cash payments, data migration, facilities, and knowledge transfer. These TSAs will not exceed [duration of the transitional agreements] in duration, except [specific support for the Purchaser]. The TSAs that Synopsys commits to enter into relate to the following:

- [Support the Purchaser during the transition to its own licensing system].
- [Support the Purchaser during the transition to its own software delivery system].
- [Transitional support for misdirected cash payments].
- [Transitional IT services].
- [Transitional use of certain physical facilities].

[9] These four individuals also prominently feature in the Confidential Information Memorandum shared with interested purchasers of the OSG Divestment Business.

- [Assistance in relation to data migration][10]
- [Assistance in relation to knowledge transfer][11]

3. The Divestment Business shall not include:

3.1 The OSG Divestment Business utilizes the following facilities, personnel and products which are not included in the Divestment Business:

- **Facilities.** [Number of] OSG Divestment Business, will (i) be provided with stand-up alternative office locations by the Purchaser, or (ii) be offered to work remotely or (iii) at other facilities determined by the Purchaser.
- **Synopsys Enterprise Software.** [Synopsys will support the Purchaser during the transition to its own licensing and software delivery systems].
- **Personnel.** The OSG Divestment Business currently relies on a limited number of employees for certain marketing and communications and back-office services. Functions provided by these employees will be seamlessly provided by equivalent personnel already at the disposal of the Purchaser.
- **Certain Shared Customer Contracts.** [Description of the customer contracts shared between Synopsys and the OSG Divestment Business and commitments on the division of contracts to ensure service continuity]. [12]
- **Shared Vendor Agreements**. [Description of the vendor agreements shared between Synopsys and the OSG Divestment Business and commitments to ensure service continuity]. [13]
- **Back-office services.** The following back-office services provided by the wider Synopsys business are not included in the OSG Divestment Business: IT & cybersecurity, finance (including order management), facilities management, corporate marketing services, legal, and HR.

3.2 **Source Code of Retained Products**. [Transitional arrangement provisions to ensure that customers of the OSG Divestment Business continue to benefit from interoperability with relevant Synopsys retained products, without requiring Synopsys to disclose its proprietary source code].

3.3 [Information on the existing interoperability between the OSG Divestment Business and Synopsys retained products and confirmation that the interoperability is not material to the viability of the OSG Divestment Business].

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10 [Information on the duration of transitional agreements related to the divestment].

11 [Information on the duration of transitional agreements related to the divestment].

12 Post-divestment, [transferred technology] would belong entirely to the OSG Divestment Business Purchaser and would no longer be sold by Synopsys.

13 [Information on shared vendors].

3.4 [Information on the data-exchange mechanisms adopted to maintain interoperability between the OSG Divestment Business and relevant Synopsys retained products, without requiring Synopsys to disclose its proprietary source code].[14][15]

4. If there is any asset or personnel which is not covered by paragraph 2 of this Schedule but which is both used (exclusively or not) in the Divestment Business and necessary for the continued viability and competitiveness of the Divestment Business, that asset or adequate substitute will be offered to potential purchasers.

[14] During this period, Synopsys and the Purchaser will use best efforts to continue to agree on implementing a new mechanism to maintain the current interoperability [information on transitional agreements related to the OSG Divestment Business].

[15] Synopsys commits that the transitional agreements will ensure that shared customers of Synopsys and the OSG Divestment Business can seamlessly continue their ongoing design projects [information on transitional agreements related to the OSG Divestment Business]. Shared customers will retain access to all designs and intellectual property created using Synopsys and OSG tools.

SCHEDULE II – PCA DIVESTMENT BUSINESS

1. The Divestment Business as operated to date has the following legal and functional structure: The Divestment Business (also referred to as the "PCA Divestment Business") currently sits within Ansys' Semiconductor Business Unit and is comprised of Ansys' global register-transfer level ("RTL") Power Consumption Analysis business and associated assets as described herein.

2. In accordance with paragraph 8 of these Commitments, the Divestment Business includes, but is not limited to:

(a) The following main tangible assets: *Not Applicable.*

(b) The following main intangible assets:

- **Patents:** Ansys commits that all patents exclusively or predominantly used by the PCA Divestment Business will be transferred. A list of patents pertaining exclusively to the PCA Divestment Business are set out in **Schedule II – Annex I.**

- **Intellectual Property:** the PCA Divestment Business will include (by way of assignment or license) all assigned and licensed intellectual property currently used by, and required to allow the PCA Divestment Business to continue operating as it does today.[16] This includes [list of software rights, quality assurance systems for code testing, domain names, and IP related to the PCA Divestment Business].[17]

- **Brands / Trademarks:** The PCA Divestment Business does not have any registered brands / trademarks. The Notifying Party and/or Ansys will, however, assign / transfer to the Purchaser any common law rights relating to the *PowerArtist* name.

(c) the following main licenses, permits and authorisations: *Not Applicable*.

(d) the following main contracts, agreements, leases, commitments and understandings:

- **Customer contracts**: the PCA Divestment Business includes customer contracts that are exclusively related to the PCA Divestment Business, which will be transferred in their entirety (including IP protection rights, pricing terms, *etc*.) to the Purchaser subject to the consent of the applicable customer if required. "Shared customer contracts" include services that are both provided by the PCA Divestment Business and other businesses of Ansys more broadly. [Information on customer contracts shared between Ansys and the PCA Divestment Business]. Specifically, Ansys will use best efforts to support the Purchaser to enter into new agreements with relevant customers (thus "splitting"

[16] This includes [list of utility functionalities used in a number of Ansys retained products and the rights of Synopsys and the Purchaser to use them].

[17] This includes the intellectual property set out in **Schedule II – Annex II**.

the relevant contracts). The IP and pricing provisions will be negotiated alongside any other terms of the shared customer contracts in the course of the Purchaser entering into new agreements with those customers. A representative list of PCA Divestment Business customer contracts is set out in **Schedule II – Annex III**.

Of the shared customer contracts identified to date, [information on customer contracts shared between Ansys and the PCA Divestment Business] and, as described above, Ansys and Synopsys will use best efforts and cooperate in good faith to facilitate the execution of new contracts between the Purchaser and the applicable customer, or to otherwise assign, sub-contract or otherwise delegate the relevant PCA Divestment Business portion.

- **Interoperability Agreements.** With respect to interoperability agreements related to the PCA Divestment Business, the relevant portions of such agreements will be divested and transferred in their entirety to the Purchaser, or Ansys and Synopsys will use best efforts to assist the Purchaser in entering into new agreements with the applicable counterparties.

- **Vendor Agreements**: the PCA Divestment Business includes vendor contracts exclusively related to the PCA Divestment Business, which will be transferred subject to the consent of the applicable vendor. The PCA Divestment Business also includes vendor contracts related to the PCA Divestment Business that also relate to the retained business, *i.e.*, ("shared vendor contracts"). With respect to such shared vendor contracts, the Notifying Party and Ansys will use best efforts and cooperate in good faith with the Purchaser to facilitate the execution of a new contract between the Purchaser and the applicable vendor, or Ansys will transfer its rights in such vendor contract to the extent related to the PCA Divestment Business to the Purchaser. A representative list of vendor contracts is set out in **Schedule II – Annex IV**.

(e) the following customer, credit and other records: *Not Applicable*.

(f) the following personnel:[18]

- The PCA Divestment Business will include at least [number of personnel] personnel across Product Management, R&D, and Application Engineering functions.[19]

[18] An overview of the Key Personnel and other personnel transferring with the PCA Divestment Business is set out at **Schedule II – Annex V**. For the avoidance of doubt, all personnel required to effectively operate the PCA Divestment Business will transfer with the PCA Divestment Business.

[19] The roles embodied by these individuals are capable of effectively operating the PCA Divestment Business as a standalone, competitive business from the outset. In any event, the total number of transferring Personnel will not exceed [information on number of personnel to be included in the PCA Divestment Business].

- This includes [number of personnel] Application Engineering personnel needed to support *PowerArtist*, which are responsible for [functions of personnel] will ensure the seamless transition to the Purchaser's own sales functions.[20]

- In addition, Ansys will use best efforts to and will cooperate in good faith with the Purchaser, to identify [number of personnel] salespeople to include in the PCA Divestment Business, of which [information on location of personnel related to the divestment].[21]

(g) the following Key Personnel:[22]

- [Identity and role of Key Personnel].

(h) the arrangements for the supply with the following products or services by Ansys or Affiliated Undertakings for a transitional period (as set out below) after Closing:[23]

- **License to develop [product feature] functionality:** Ansys is currently developing a new feature in *PowerArtist* [information on product feature][24] [25] this feature will be included in the PCA Divestment Business to the benefit of the Purchaser.

  [The product feature is not part of the PowerArtist source code and is also used in an Ansys retained tool].[26]

  To enable the Purchaser to independently conduct [functionality provided by product feature] with *PowerArtist*[27] post-transition, Ansys commits to [description of separation measure] provide a license of all such relevant source code to the Purchaser on a limited-purpose, non-exclusive, royalty-free basis [28]

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20 [Information on functions of certain personnel to be included in the PCA Divestment Business].

21 [Information on the type and function of personnel to be included in the PCA Divestment Business].

22 *See* footnote 18.

23 Ansys commits that these arrangements will allow the Purchaser to continue operating the PCA Divestment Business as it is operated at Closing of the divestiture transaction without interruption and will ensure that, subject to the transfer of customer contracts, customers (including customers under shared contracts) of the PCA Divestment Business are able to [information on the nature, content and duration transitional support]. In any event, Ansys will provide to the Purchaser customer licensing services for customer product licenses, including assistance with obtaining new licenses, renewals, expansion, and upgrades, until [duration]. For the avoidance of doubt, none of these transitional links will affect the viability of the PCA Divestment Business:

24 [Description of product feature].

25 [Description of product feature development maturity].

26 [Description of product feature].

27 [Description of product feature].

28 [Description of product feature license].

Ansys will deliver the […] code within [timing] of Closing of the divestiture transaction. On a conservative basis, and based on Ansys' experience, [number of personnel] (who will be included within the Personnel transferring with the PCA Divestment Business) would be needed to support the licensed code such that it can be maintained and developed on a lasting basis..

For the transitional period until the […] source code is available, the Purchaser will be granted a limited-purpose, non-exclusive, royalty-free license to [product feature] as object code, for a period beginning upon the Closing of the divestiture transaction and continuing for [duration] following the delivery of the […] source code (the latter being deliverable within [duration] of Closing of the divestiture transaction.[29]

- **License to develop [product feature]:** Ansys has recently developed a *PowerArtist* feature [information on product feature][30].

  [Product feature] can be replaced by further developing PowerArtist's code[31] or using open-source functionality from [product feature].[31] [32] The Personnel transferred with the PCA Divestment Business have the necessary skills and experience to accomplish this. On a conservative basis, and based on Ansys' experience, a full transition to a native alternative can be accomplished [period].

  To enable a transitional period during which the Purchaser develops this functionality natively (with relevant Personnel transferred with the PCA Divestment Business), Ansys will provide a limited-purpose, non-exclusive, royalty-free license to [product feature].

- **License to develop [product feature]:** Ansys is currently developing a new feature in *PowerArtist* [description of product feature]. The Personnel transferred with the PCA Divestment Business have the necessary skills and experience to accomplish a full transition to a native alternative. Based on Ansys' own experience, and on a conservative basis, this can be done in as little as [description of product feature].

  To allow the PCA Divestment Business to natively develop *PowerArtist*'s functionalities and preserve the functionality currently available in the product, Ansys will provide a limited-purpose, non-exclusive, royalty-free license to [product feature] for a transitional period of up to [period].

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[29] Object code refers to machine-readable compiled code used to run the software. Object code is produced when a compiler translates the human readable source code to machine readable code. For clarity, this license will not provide the Purchaser with the underlying source code.

[30] For completeness, Ansys has recently developed a *PowerArtist* feature for [description of product feature].

[31] [Description of product feature].

[32] Si2 is a consortium of key semiconductor players focused on enhancing interoperability. This standard body consists of several working groups that define industry-standard formats that EDA tools generally need to comply with.

- **License to develop [product feature]:** [Description of product feature]. This technology does not form part of *PowerArtist's* foundational technology [description of product feature].

  The Personnel transferred with the PCA Divestment Business have the necessary skills and experience to develop [product feature]. Based on Ansys' experience developing similar technology and on a conservative basis, this can be transitioned within [period]. To enable a transitional period during which the Purchaser develops this functionality, Ansys will provide a limited-purpose, non-exclusive, royalty-free, object-code license to [product feature] during a transitional period of up to […].

- **License back to [product feature]:** The *PowerArtist* [product feature] source code will be included in the PCA Divestment Business.[33] Ansys will, however, require a transitional license-back of the source code for a limited period of up to [duration and transitional purpose of license]. [Following transitional steps], the license-back will no longer be needed.

- **IT – Transition and Transfer Support:** for a limited transitional period of up to [duration] following the Closing of the divestiture transaction, the Notifying Party and/or Ansys will provide certain IT and other support services to the Purchaser to facilitate the transition and migration of the PCA Divestment Business onto the IT infrastructure of the Purchaser, pursuant to a Transition Services Agreement. These services consist of standard transition support services for [duration and content of transitional services].

- **Facilities:** for a period of up to […] from the Closing of the divesture transaction, Ansys will make available transitional support with respect to the provision and maintenance of designated workspaces for PCA Divestment Business Personnel [information on facilities].

- **Knowledge Transfer:** for a period of up to […] from the Closing of the divesture transaction, Ansys will make available transitional support to facilitate knowledge transfer and PCA Divestment Business processes.

- **Finance – Accounts Receivable:** [Information on financial transitional agreements].

- **Cash Settlement:** for a period of up to […] from the Closing of the divestiture transaction, Ansys will provide to the Purchaser support for settlement of misdirected cash that is erroneously sent by PCA Divestment Business customers to Ansys' lockboxes and bank accounts.

- **Customer Licensing:** Ansys will provide to the Purchaser customer licensing services for customer product licenses, including assistance with obtaining new licenses, renewals, expansion, and upgrades, until […].

[33] [Information on product feature].

- **[Product feature]:** For the transitional period beginning upon […] [34] and for up to […] thereafter, Ansys will support the Purchaser with respect to quality assurance and other testing to ensure that the parsed source code permits the operation of the PCA Divestment Business in such manner as the PCA Divestment Business operated as of the Closing of the divestiture transaction.

- **Website Traffic Redirection:** For a period of up to […] from the Closing of the divesture transaction, Ansys will redirect website traffic for a certain PCA Divestment Business website (https://www.ansys.com/products/semiconductors/ansys-powerartist) to a website provided by the Purchaser.

- Ansys and the Purchaser will enter into a customary arrangement whereby (i) Ansys will agree not to enforce its retained IP rights (as they exist as of the time of Closing) against the Purchaser in order to prevent it from operating the PCA Divestment Business, and (ii) the Purchaser will agree not to enforce IP rights transferred with the PCA Divestment Business (as they exist as of the time of Closing) against Ansys in order to prevent it from operating its retained business, to the extent any such rights are used in or necessary for the operation of the retained business' activities unrelated to the activities of the PCA Divestment Business. Any such customary arrangement will be set out in the final binding sale and purchase agreement and will be subject to the assessment by the Monitoring Trustee and the Commission's prior approval.

3. The PCA Divestment Business shall not include:

(a) **Intellectual Property**: please refer to **Schedule II – Annex II** for a list of excluded intellectual property.

(b) **Facilities**: [Information on facilities not included in the Divestment Business.]

(c) **Tangible Personal Property**: The PCA Divestment Business will not include tangible personal property (other than the laptop and desktop computers used by employees of the PCA Divestment Business, if the Purchaser notifies Ansys in writing of its election to include such assets prior to the Closing of the divestiture transaction) as the requisite hardware will be available at the Purchaser unless specifically requested by the Purchaser in which case any relevant hardware will be included in the PCA Divestment Business.

(d) **Corporate IT**: The PCA Divestment Business currently leverages a corporate IT infrastructure (encompassing both hardware and software) that is shared across the PCA Divestment Business and Ansys' other businesses. Ansys will make available transitional support allowing the PCA Divestment Business to migrate seamlessly onto the Purchaser's systems.

(e) **Non-dedicated employees**: For completeness, **Schedule II – Annex VI** provides an overview of employees that are not being transferred as part of the PCA Divestment Business but that currently serve the PCA Divestment Business to a limited degree.

[34] The [product feature] shall be deliverable within [period] of Closing of the divestiture transaction.

These individuals all perform an Application Engineering function, and less than 40% of their time is dedicated to the PCA Divestment Business.[35]

4. If there is any asset or personnel which is not covered by paragraph 2 of this Schedule but which is both used (exclusively or not) in the Divestment Business and necessary for the continued viability and competitiveness of the Divestment Business, that asset or adequate substitute will be offered to potential purchasers.

[35] Ansys commits that any internal restructuring of the PCA Divestment Business will not have an impact on its viability, including the Key Personnel. All Key Personnel (and more generally, all Personnel), for example, are being offered an attractive retention incentive scheme, consistent with paragraph 10(c) above.